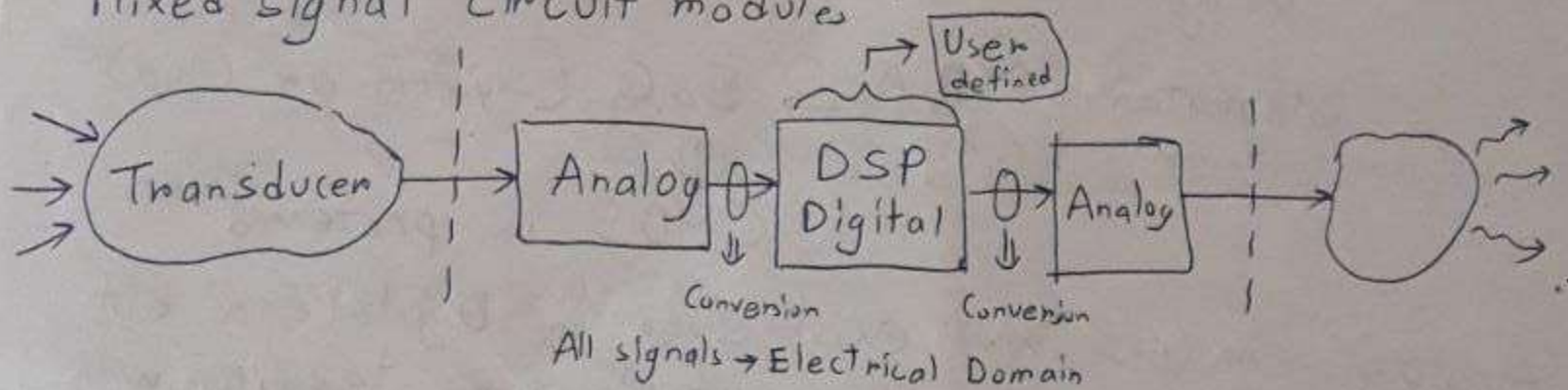
1/9/20 (Week 1)

Evaluation → Once in 2 weeks
→ Depends on previous week (1, 2) contents

Books :-
1) CMOS Analog Circuit Design
↳ Allen, Holberg
2) Design of Analog CMOS ICs
↳ Razavi
3) Analog MOS
↳ Temes
4) Art of Analog Layout
↳ Alan Hastings

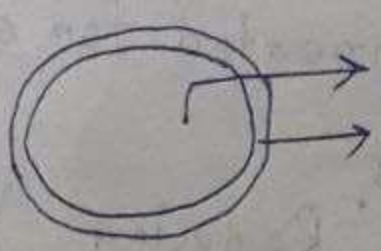
- Electronic system containing Analog, Digital and Mixed signal circuit modules

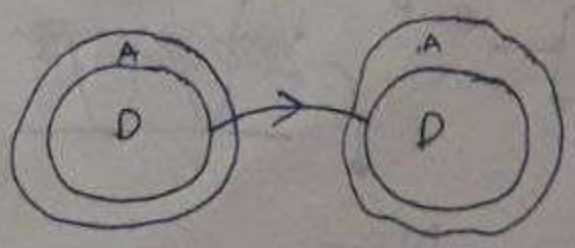



All signals → Electrical Domain

Analog: Interfacing with external world (real world) [Peripheral]
Digital: Core Processing
→ Flexibility, programmability, scope of expansion
→ Compact storage and Low power
→ Successful progress of supporting technology [Business driven]

Analog → Limited scope, very low flexibility

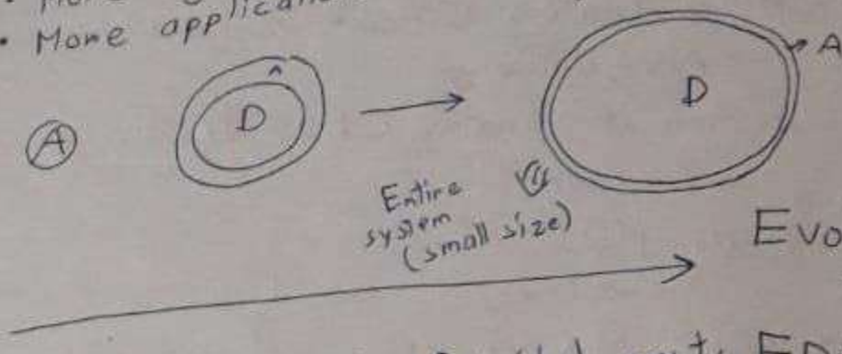



Info Tx. (digital data)
But analog - analog interface is restricted.

Analog will never cease to exist, but periphery module will reduce in size, as processing is desired only in digital.

Evolution of electronic systems: [size → Complexity]
- More digitization with time
- More applications and integration




Design of Digital part: EDA (Electronic Design Automation)
↳ Computer design

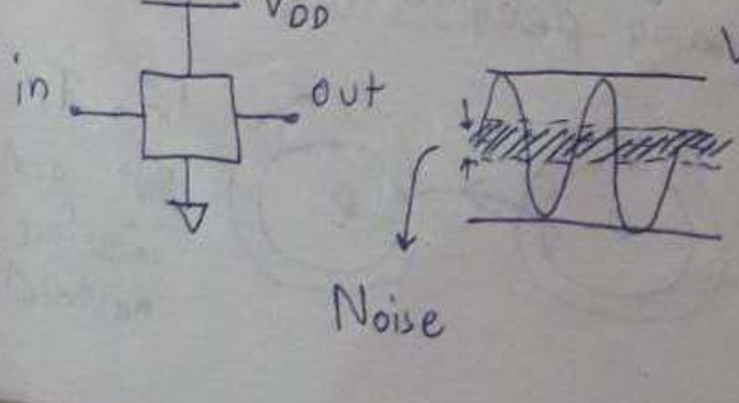
Design of Analog part: Custom / Human design

Integration of D, A on 1 chip → SoC (System on Chip)
⇓
CMOS is preferred

Analog circuits will exist even in Digital era but in evolved formats. It is suitable for integration with digital counterpart.

Challenges →
- Reduced supply voltage
- "Poor" Intrinsic Gain of MOSFET
- Limited Passive Components
- Variations in PVT.

(1) $P_{diss} \downarrow \Rightarrow V_{supp} \downarrow \Rightarrow$ Devices also become smaller in size
↳ (Not much recommended for analog)

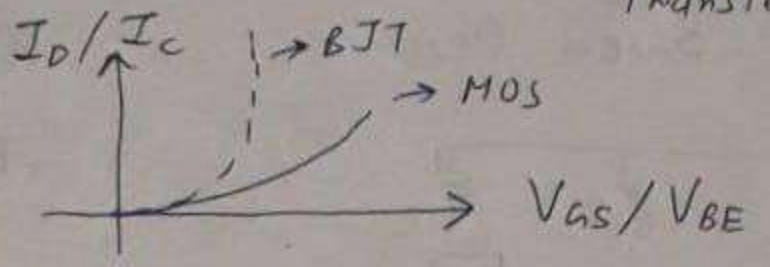



Reducing $V_{supp}$,
- reduces swing and affects signal quality (SNR).

(2) BJT → Intrinsic gain = $g_m r_o$

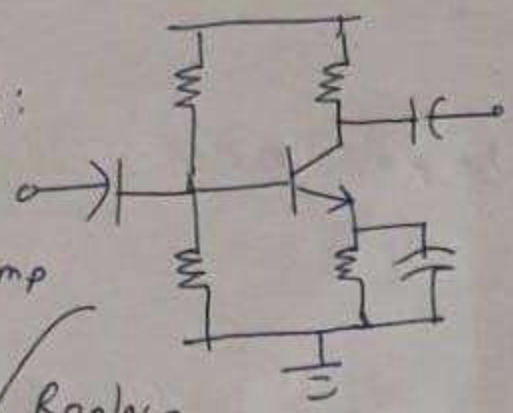
$g_m$ of BJT is very high due to exp. transfer cha.

$g_m$ of MOS is much lower due to square root transfer characteristic

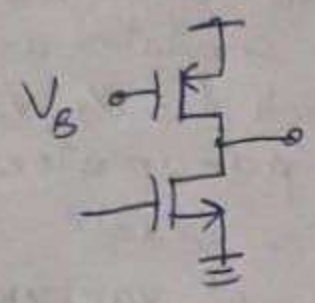



Hence it is Challenge. ↓ Make topological advantages.

(3) In analog circuits: (4th sem)

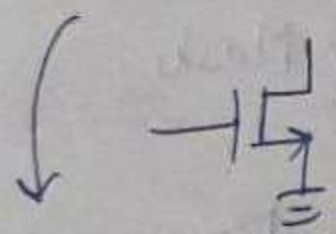



1 active
Rest all passive
↓
Very problematic for on chip.




CS amp. with active load [Reduces no. of passive gain] ∴ ↳ Gives back the req d. gain

(4) PVT → Process, Voltage, Temp.




Circuit has to work with this deviations as well.

Direct influence of yield

Poor Yield: Lower no of functional device

$V_{dd}\downarrow \Rightarrow$ Scale down and variation → Challenge

Flow of course:-

1) Analog building blocks:- Primary desi
   - Working principles
   - Analysis and Design / Sizing (W, L) ??

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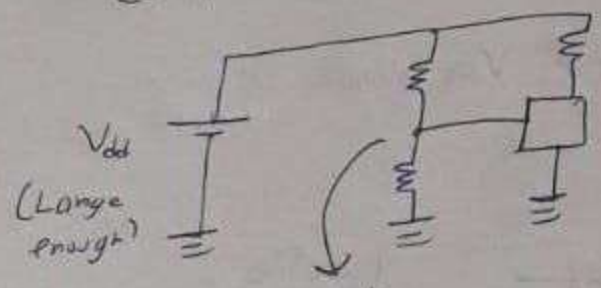
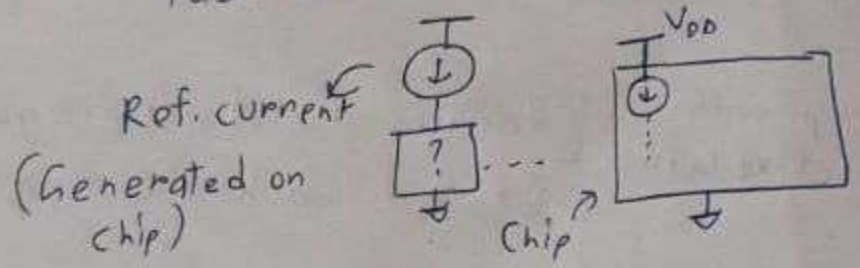
# Course Layout

Component Based Design




Wont to change? → Use potentiometer

↳ We know IV char. of already fab. device




VLSI (Sensitive)

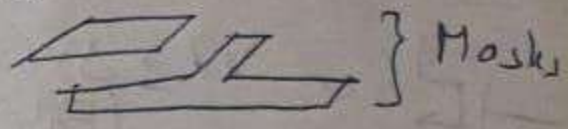
↓

- Every component sized $V_{dd} \sim 4 V_{TH}$
- No resistors

↳ Special bias circuitry needed

↳ We have some uncertainity in components (W, L) and char. → Use simulation and check for % variation in parameters and thus stable performance irr. of variation

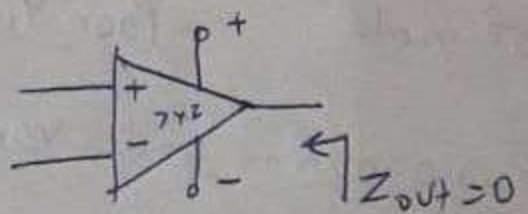
Layout: Topology & W, L ⇒ Polygon mask layers




OTA / Opamp

↓

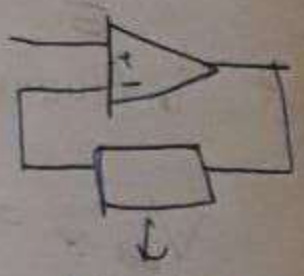
IC-741




$Z_{out}(Opamp) = 0$

⇓

Voltage form output

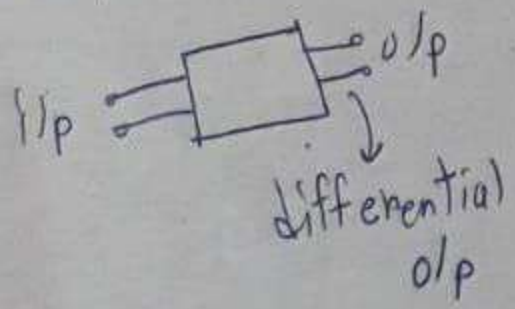


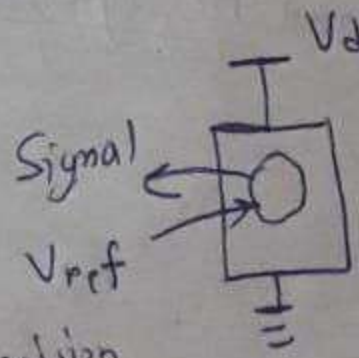

$Z_{out}(Opamp) = \infty$

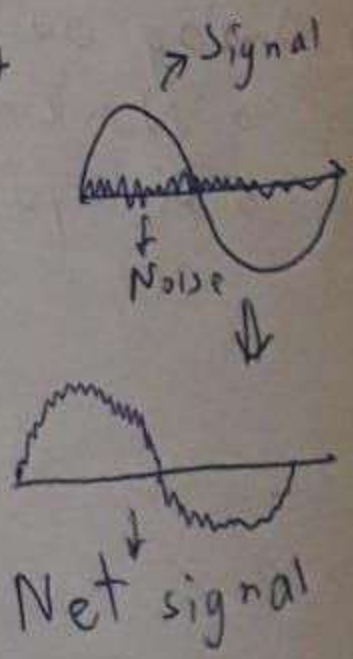
⇓

Current form output

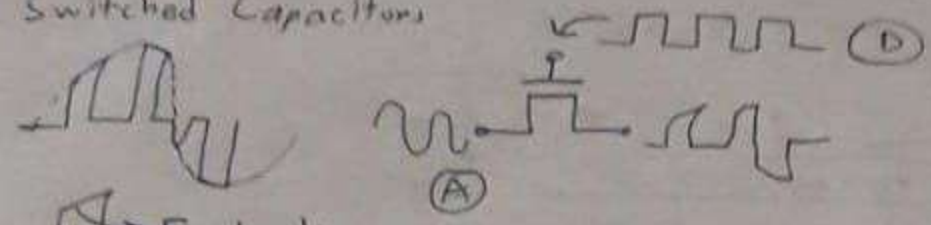
Fully differential amp.



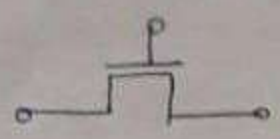



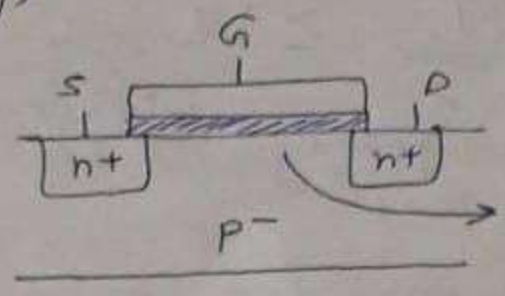



Switched Capacitors

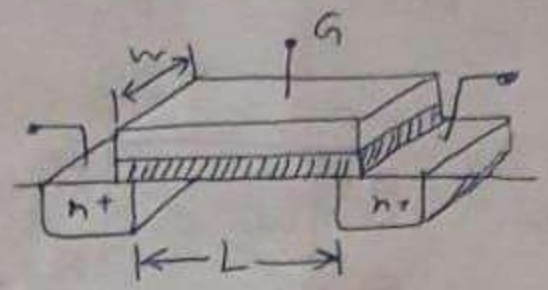



## MOSFET (Geometry)




Oblique view:




In VLSI, we find values of W and L.

Exam → Next week onwards

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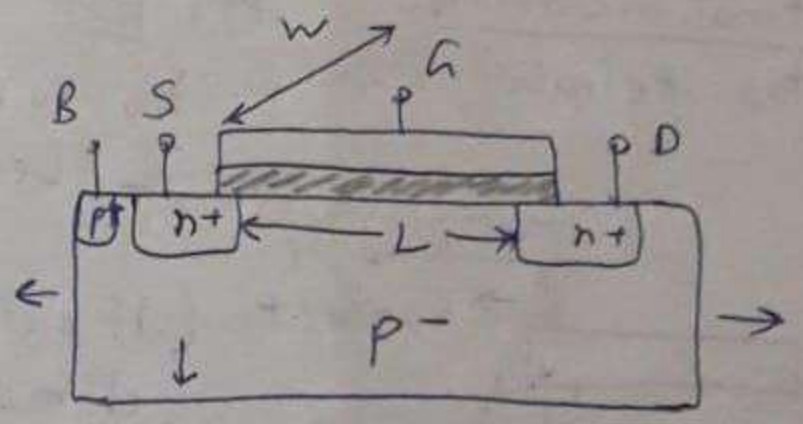
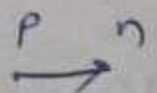
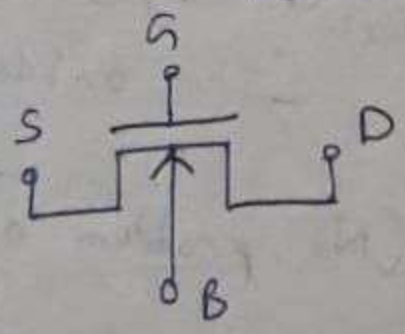
Ideal Cross-section view →




↓

All connections are shown as stick




p+ Pocket → Avoid Schottky diode formation [Make Ohmic Contact]

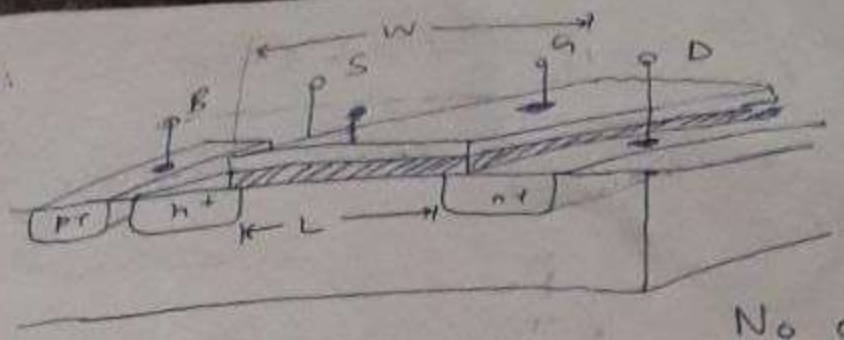
S, D are interchangable

nMOS: Current flows D → S ($V_D > V_S$)

Carriers ($e^-$) flow S → D [n channel]

Higher potential ⇒ Drain (nMOS)

Oblique view:




No control on oxide thickness, well depth.
[Process parameters]

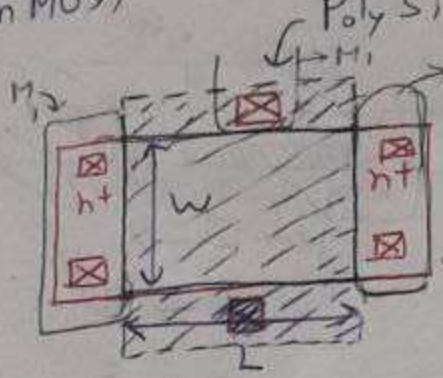
B → Need not be extended in width.

$W, L \geq W_{min}, L_{min}$ [Process]

↓

Designer's play

Top view: (nMOS)




We extend the gate material beyond channel (up and down)

Boundary n+ zones are aligned with channel.

↓

Self-aligned process

→ active (includes below gate region)

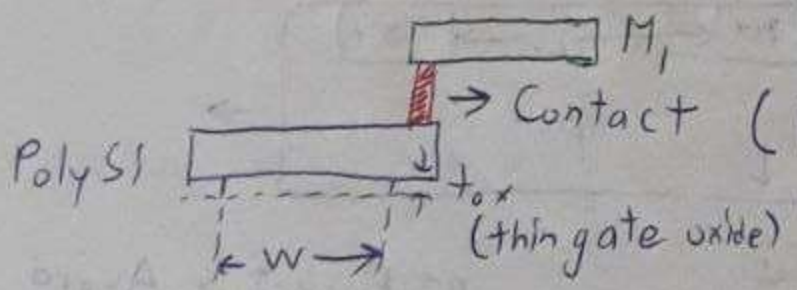
Mask layers:
- → active
- → Contact
- → Metal 1 ($M_1$)
- poly

* Contact not on channel.

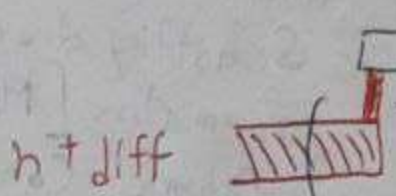
↳ Creates reliability issues

W: Width of active region

L: Length of poly Si channel




(If on channel, it damages the device)
[Thin oxide]




(No problem as no oxide is present)

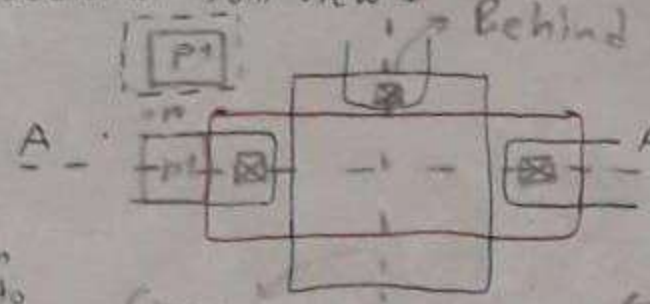
In between we have $SiO_2$ (thick field oxide)

$M_1 - M_2$ : Via 1  M - M : Vias

$V_B$ → Lowest pot. (RB diode) $V_{SB} > 0$

Active region: Drain, Source diff. + Channel

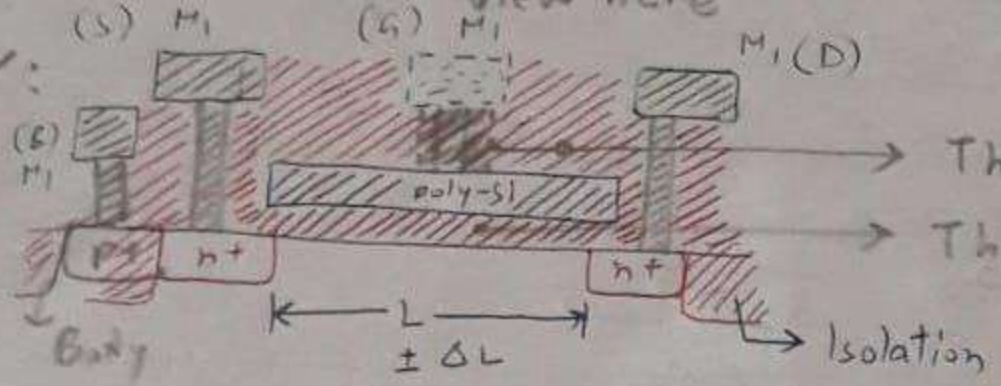
Cross-sectional front view



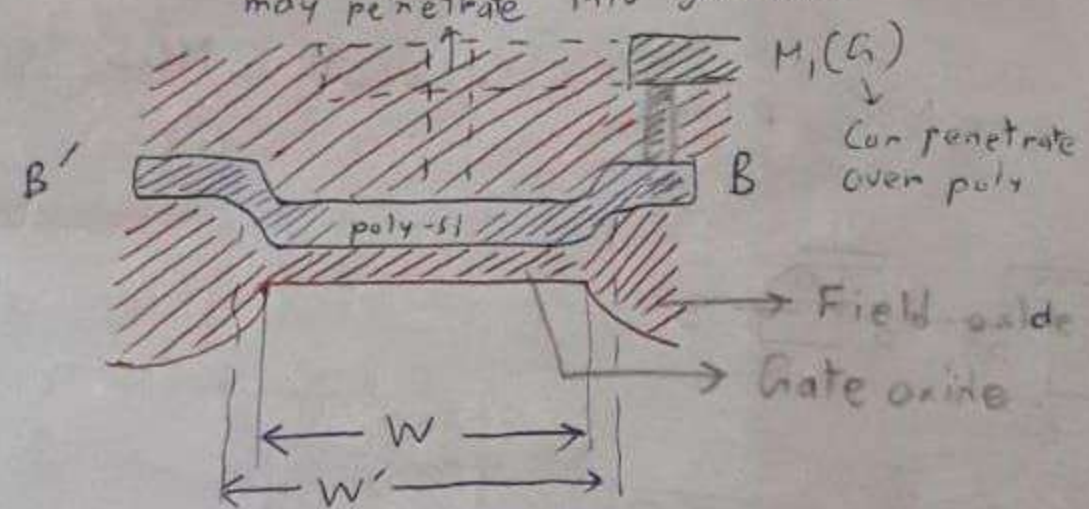

$p^+$, $n^+$ → can be close to each other

(Cross section) View here ← View here

AA':




BB':



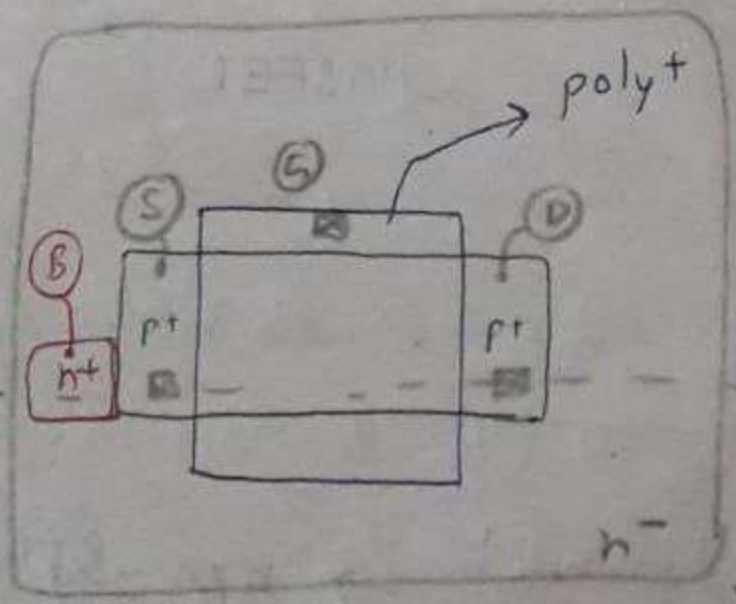

Field oxide
↳ Mechanical strength
↳ Electrical isolation
↳ Keep L, W const.

$W' = W \pm \Delta W$ (Bird's beak effect)

ΔL, ΔW
↓
Foundry limitations

No need for dedicated body for every device

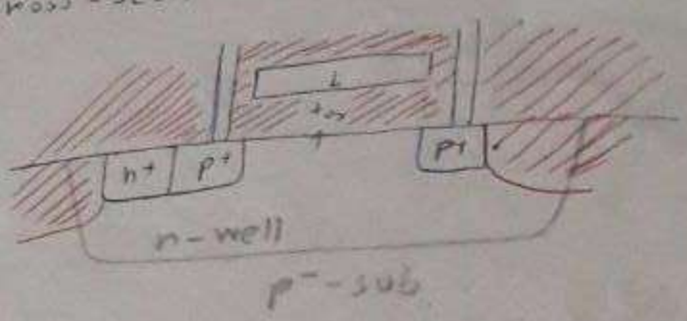
pMOS:
↓
$V_S \geq V_D$
$V_B$ → Highest pot.
(RB diode)
$V_{BS} > 0$




Self aligned
↓
Gate is exposed to diffusion.

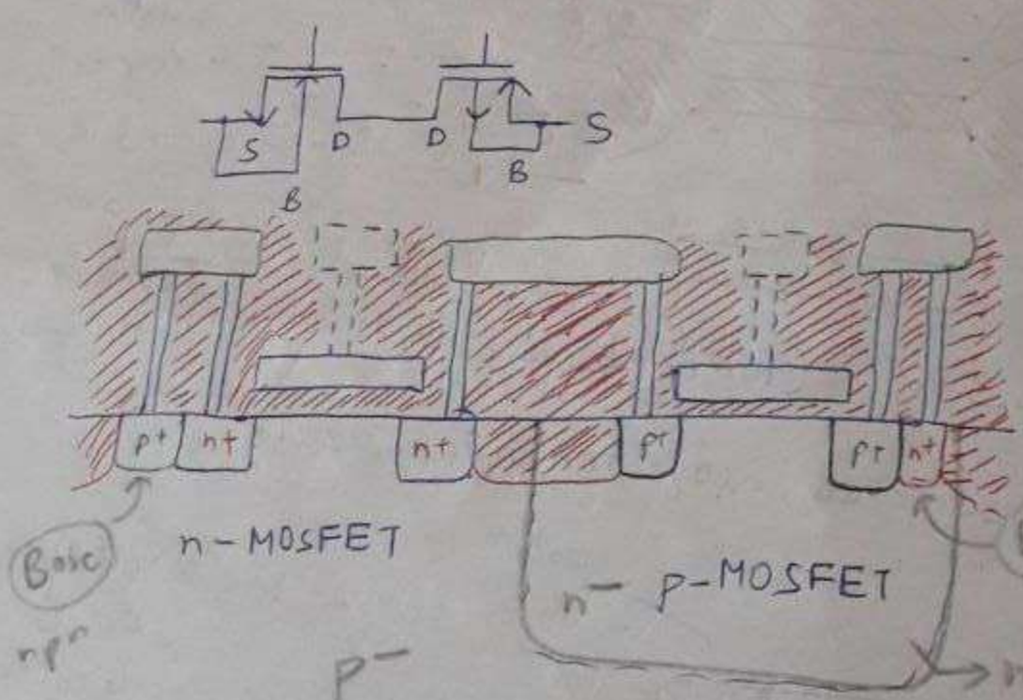
$poly^+$ → PMOS ($N_a$)
$poly^-$ → NMOS ($N_d$)

Cross-sectional view:



P → n

[Practice: nMOS, pMOS in n-well CMOS tech.]

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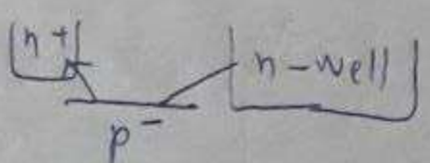
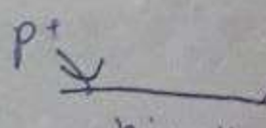



→ npn-BJT



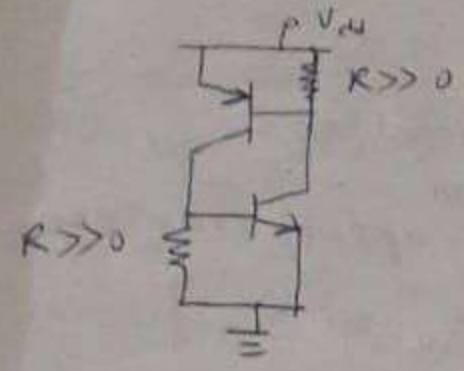

→ pnp BJT

→ Latch up circuit

⇓

Remove them by keeping nMOS, pMOS wide.

∴ More base contacts, farther n and p regions → parasitic BJTs $V_{BE} = 0$ → Shorted [∴ Reduction in latchup]




R>>0
↳ BJTs help and make direct short b/w $V_{dd}$ and 0.
↳ R is made low by making more base contacts, higher spacing/ isolation.

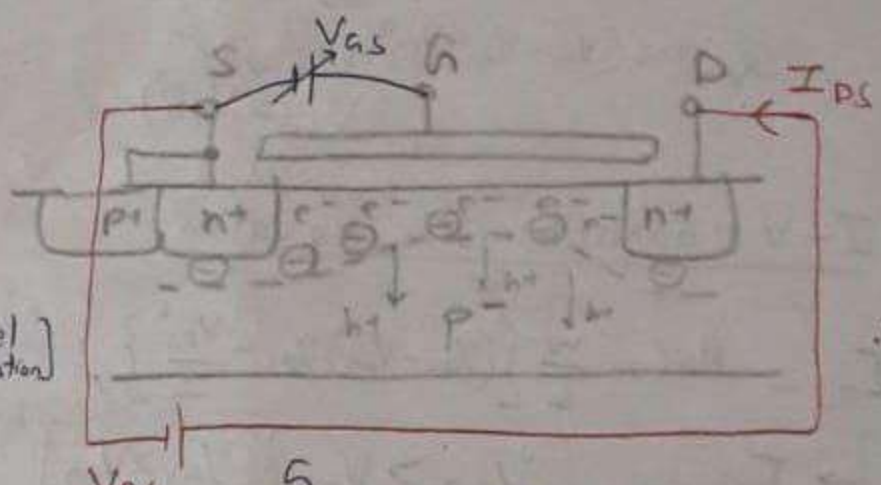
7/9/20 (Week-2)

Assignment 1 (Deadline): Tuesday Midnight

## Operating Principle of Enhancement n-MOS

$V_{GS} > 0$
↳ Formation of depletion layer (holes repelled)

$V_{GS} > V_{th}$ (Threshold) [Channel formation]
↳ Electrons accumulate
[$e^-$s from $p^-$ (minority) and $e^-$s from $n^+$ Source]
[Depleted donors + Electrons]




What is $V_{th}$? [Min. voltge at ↗] $e^-$ conc. in channel = $h^+$ conc in bulk

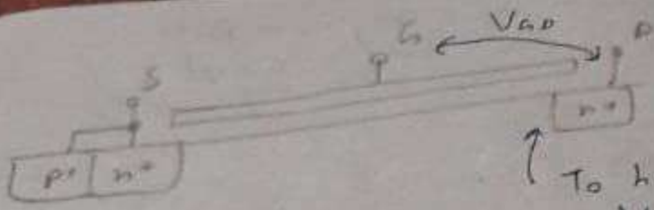
As $V_{GS} - V_{th}$ increases: stronger channel b/w D and S.
↳ More charge accumulated

Now we apply $V_{DS}$ to allow lateral movement of $e^-$s from S to D [Current $I_{DS}$].

Might be controlled by $V_{SB}$ ↑ ; $\frac{\epsilon_{ox}}{t_{ox}}$ ↑

$$I_{DS} = f(\underbrace{V_{GS}, V_{DS}}_{\text{Electrical parameters}}, \underbrace{V_{th}, W, L, C_{ox}, \mu_n}_{\text{Device parameters}})$$

[Changeable] [Static]

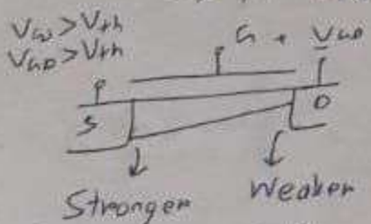



$V_{GD} = V_{GS} - V_{DS}$

↑ To have channel here
$V_{GD} > V_{TH}$

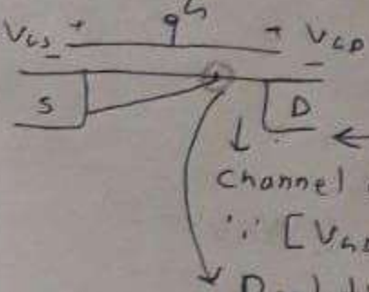
→ If $V_{GD} < V_{th}$, Channel will disappear near drain

$V_{GS} > V_{th}$
$V_{GD} > V_{th}$




[Channel exists]

$V_{GS} > V_{th}$ (Pinchoff)
$V_{GD} < V_{th}$

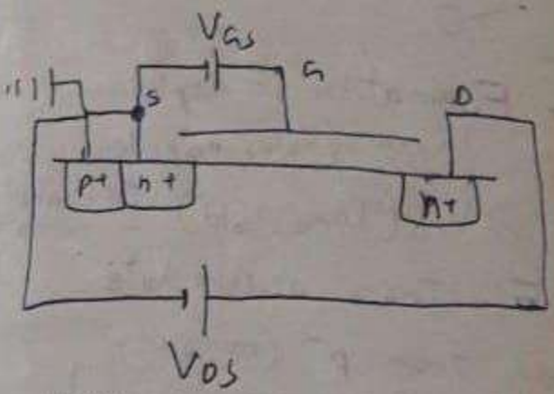



Channel disappears
$\because [V_{GD} < V_{th}]$

Depletion region [Strong field will drift e⁻s to drain]

At pinchoff point ↓
Surface potential $V(x)$
$Q_d(x) \propto (V_{GS} - V_{th} - V(x))$ is just $(V_{GS} - V_{th})$

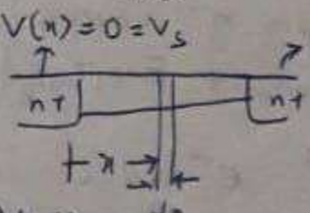
## I-V characteristic equation




$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left\{ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right\};$$

↳ Triode $[V_{GD} > V_{th}]$ $[V_{GS} > V_{th}]$

[Revise derivation]




Charge per unit length $\Leftarrow Q_d(x) = -WC_{ox}(V_{GS} - V_{th} - V(x))$

$$I = -Q_d(x) v_d \qquad v_d = -\mu_n \frac{dV(x)}{dx}$$

$$I = \mu_n C_{ox} W (V_{GS} - V_{th} - V(x)) \frac{dV(x)}{dx}$$

$$\Rightarrow \int_0^L I \, dx = \int_0^{V_{DS}} \mu_n C_{ox} (V_{GS} - V_{th} - V(x)) dV(x)$$

$$\Rightarrow I \cdot L = \mu_n C_{ox} W \left[ (V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\Rightarrow I = \mu_n C_{ox} \frac{W}{L} \left[ V_{GS} - V_{th} - \frac{V_{DS}}{2} \right] V_{DS}$$

[Derivation valid in triode where channel is (cont.)]

Limiting case: $V_{GD} = V_{th}$

$\Rightarrow V_{GS} - V_{DS} = V_{th}$

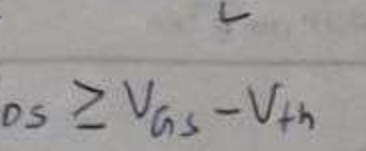
$\Rightarrow V_{DS} = V_{GS} - V_{th} = V_{Dsat}$

$\therefore \boxed{I_{Dsat}[V_{DS} = V_{GS} - V_{TH}] = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2}$ → Saturation
- $V_{GS} > V_{th}$
- $V_{GD} < V_{th}$

$[V_{DS} \geq V_{GS} - V_{th}]$

Current gets saturated here

$I_{Dsat}$




$L'$ or $L_{eff} = L - \Delta L$

($\Delta L$ small enough compared to $L$)

Most frequently used in analog circuits

To capture length shrinkage (channel length modulation):

[Effect of $V_{DS}$]

$$\boxed{I_{DS} = I_{Dsat}(1 + \lambda V_{DS})}$$

** $\lambda \propto \frac{1}{L}$ (smaller/submicron device → Prominent effect)

$V_{DS} \uparrow \Rightarrow L_{eff} \downarrow$ [$V_{DS}$ modulates eff. length]

Why B not shorted with D? $\Rightarrow$ $V_D > V_S$

↳ $V_{DB} > V_{SB}$ (More leakage)

and $V_{DB}$ → shorted

$\Downarrow$

$V_{SB} < 0 \Rightarrow$ SB diode forward bias

## Large signal I-V chara. equation:-

$$I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{th})^2$$

$$\frac{1}{L_{eff}} = \frac{1}{L - \Delta L} = \frac{1}{L(1 - \frac{\Delta L}{L})}$$

$$= \frac{1}{L}\left(1 - \frac{\Delta L}{L}\right)^{-1}$$

$$\approx \frac{1}{L}\left(1 + \frac{\Delta L}{L}\right)$$

$$\frac{\Delta L}{L} = \lambda(V_{DS} - V_{Dsat}) = \frac{1}{L}(1 + \lambda(V_{DS} - V_{Dsat}))$$

$$\boxed{I_{DS} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})}$$

↳ $V_{DS} \geq V_{GS} - V_{th}$

↳ $V_{GS} \geq V_{th}$

$\mu_n C_{ox} = K_N'$ [Transconductance parameter]

Actually it is $\lambda(V_{DS} - V_{Dsat})$ → for simplicity $1 + \lambda V_{DS}$

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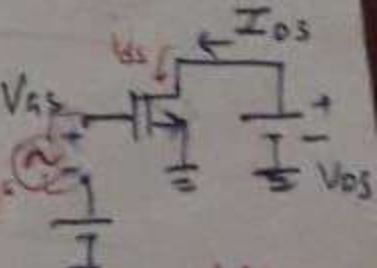
$$I_{DS} = \frac{K_n'}{2} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}); \quad [V_{DS} \geq V_{Dsat}]$$




$v_{gs}$ → small variation

$$I_{ds} = \frac{K_n'}{2} \frac{W}{L} \{(V_{GS} + v_{gs}) - V_{th}\}^2 (1 + \lambda V_{DS})$$

$v_{gs} \downarrow i_{ds}$

$V_{gs} = V_{GS} + v_{gs}$

↳ inst. voltage

$I_{ds} = I_{DS} + i_{ds}$

inst. DC small-signal

Small Signal Characteristic Equation

$$\Rightarrow I_{ds} = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{th})^2(1+\lambda V_{DS})\left[1+\frac{2v_{gs}}{(V_{GS}-V_{th})}+\frac{v_{gs}^2}{(V_{GS}-V_{th})^2}\right]$$

For simplicity, we consider $v_{gs}$ negligible.

$$\left[\frac{v_{gs}}{V_{GS}-V_{th}} \ll 1\right]$$

$$\Rightarrow I_{ds} = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{th})^2(1+\lambda V_{DS})\left[\underbrace{1}_{I_{DS}}+\underbrace{\frac{2v_{gs}}{V_{GS}-V_{th}}}_{i_{ds}}\right]$$

$\therefore i_{ds} = I_{ds} - I_{DS}$

$$= (I_{DS})\cdot\frac{2v_{gs}}{V_{GS}-V_{TH}}$$

$$= \left(\frac{2I_{DS}}{V_{GS}-V_{TH}}\right)v_{gs} \longrightarrow \text{also } g_m$$

$$i_{ds} = K_n'\frac{W}{L}(V_{GS}-V_{th})(1+\lambda V_{DS})\,v_{gs}$$

↳ Linear relation

$$i_{ds} = g_m v_{gs}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}\bigg|_{(I_{DS},V_{GS})} = \frac{i_{ds}}{v_{gs}}$$

$g_m$ : Transconductance

$K_n'$ : Transconductance parameter

* $\boxed{g_m = K_n'\frac{W}{L}(V_{GS}-V_{th})(1+\lambda V_{DS})}$ — (1)

* $\boxed{g_m = \frac{2I_{DS}}{V_{GS}-V_{TH}}}$ — (2)

* $\boxed{g_m = \sqrt{2I_{DS}K_n'\frac{W}{L}(1+\lambda V_{DS})}}$ — (3)

(1) : $(V_{GS} - V_{TH}) \uparrow \Rightarrow g_m \uparrow$ Contradictory ??

But (2) : $(V_{GS} - V_{TH}) \uparrow \Rightarrow g_m \downarrow$

(1): $\left(\frac{W}{L}\right) \uparrow \Rightarrow g_m \uparrow$ (Linear)

But (3): $\left(\frac{W}{L}\right) \uparrow \Rightarrow g_m \uparrow$ ( Root dependence) Again contradictory ??

(2): $\left(\frac{W}{L}\right) \uparrow \Rightarrow g_m$ (No dependence)

Catch → We are also assuming that $I_{DS}$, $\frac{W}{L}$, $V_{GS} - V_{TH}$ are such that they are interdependent.

V.V. Imp.

(1) $\frac{W}{L} \uparrow \Rightarrow g_m \uparrow$ (Only when $(V_{GS} - V_{TH})$ is constant)
(Linear)

↓

$I_{DS}$ has to increase linearly

(3): $\frac{W}{L} \uparrow = g_m \uparrow$ (Only when $I_{DS}$ is constant)
(sqrt)

↓

$(V_{GS} - V_{TH})$ decreases by root dependence

∴

Circuit designer aim: High $g_m$

More $g_m$ : Small change in $V_{gs}$ => High change in $I_{ds}$.

$\boxed{i_{ds} = g_m v_{gs}}$ → Small signal char. eqn.

$$I_{ds} = \frac{k_n'}{2} \frac{W}{L} (V_{gs} - V_{tn})^2 (1 + \lambda V_{ds})$$

↑ Dependency exists on $V_{ds}$

Modify →

$$\boxed{i_{ds} = g_m v_{gs} + g_o v_{ds}}$$

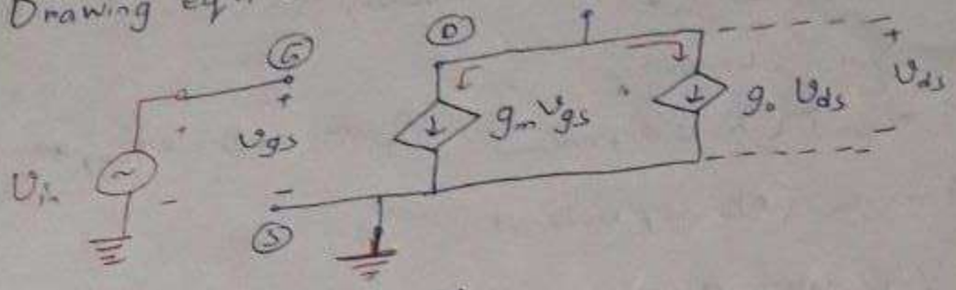
- $g_m v_{gs}$ : Diff. port ↓ transfer conductance
- $g_o v_{ds}$ : Same port => o/p conductance

$$g_m \triangleq \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{(I_{DS}, V_{GS}, V_{DS})}$$

$$g_o \triangleq \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{(I_{DS}, V_{GS}, V_{DS})}$$

## Small Signal Equivalent ckt

Drawing eqv. ckt. →



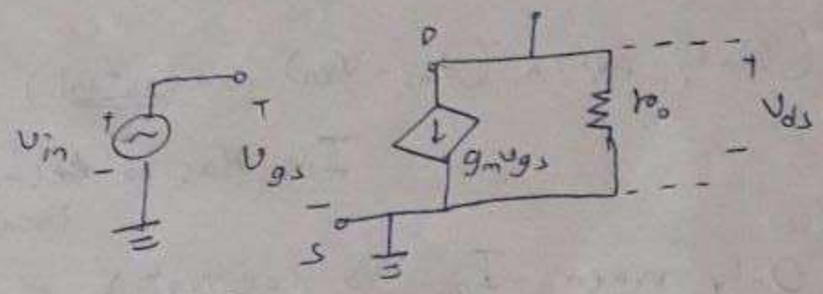

B connected to source

Fin

$\Downarrow$

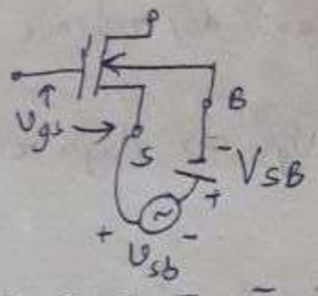
$g_o v_{ds}$ across $v_{ds}$ → Resistor

$r_o = \frac{1}{g_o}$




Ex

Body - Source (diff. pot.)




$V_{SB} + v_{sb} = V_{sb}$

↓

Influence on channel behaviour

$$V_{th} = V_{th0} + \gamma\left[\sqrt{V_{sb} + 2|\phi_F|} - \sqrt{2|\phi_F|}\right]$$

$$\frac{\partial V_{th}}{\partial V_{sb}} = \frac{\gamma}{2\sqrt{V_{SB} + 2|\phi_F|}} > 0$$

$$\frac{\partial I_{ds}}{\partial V_{sb}} = \frac{\partial I_{ds}}{\partial V_{th}} \times \frac{\partial V_{th}}{\partial V_{sb}} = -\frac{g_m \gamma}{2\sqrt{V_{SB} + 2|\phi_F|}} = -g_{mb}$$

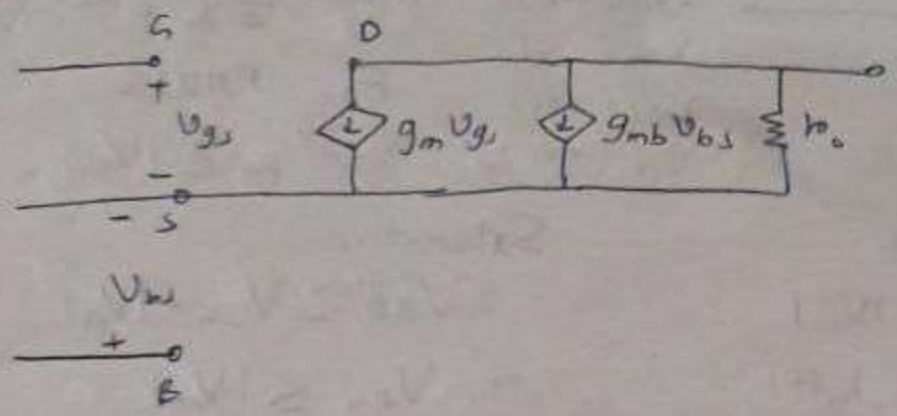
$$i_{ds} = (-g_m v_{gs}) - g_{mb} v_{sb}$$

$v_{gs} = 0$

Almost $\frac{1}{10}$th of $g_m$

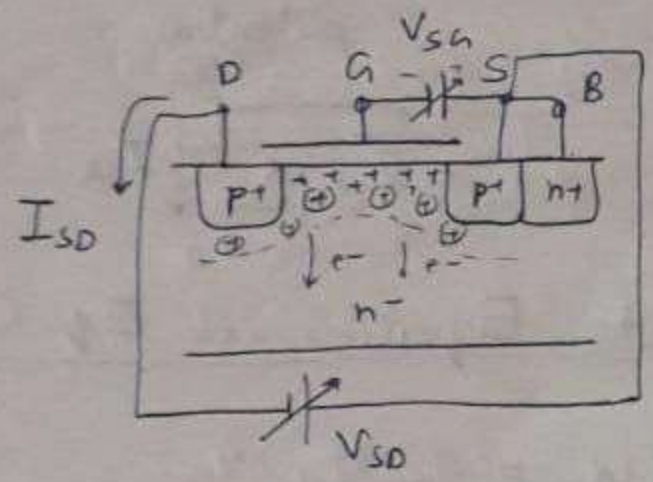
$$\boxed{i_{ds} = g_{mb} v_{bs}}$$

Final model :-

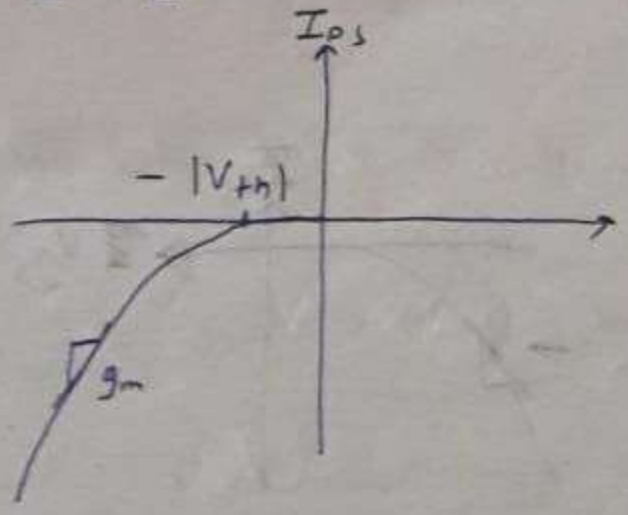



Exercise – Do the same analysis for PMOS. (Enhancement mode)

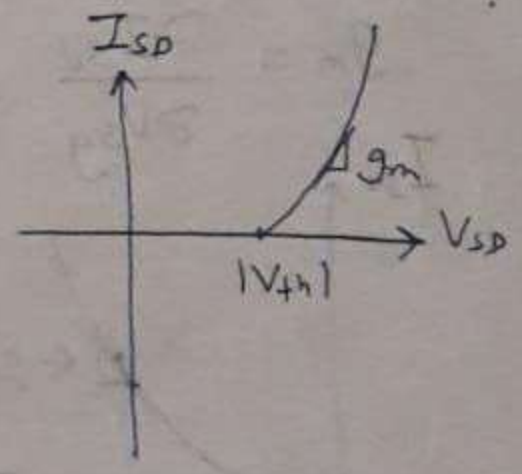
Biasing



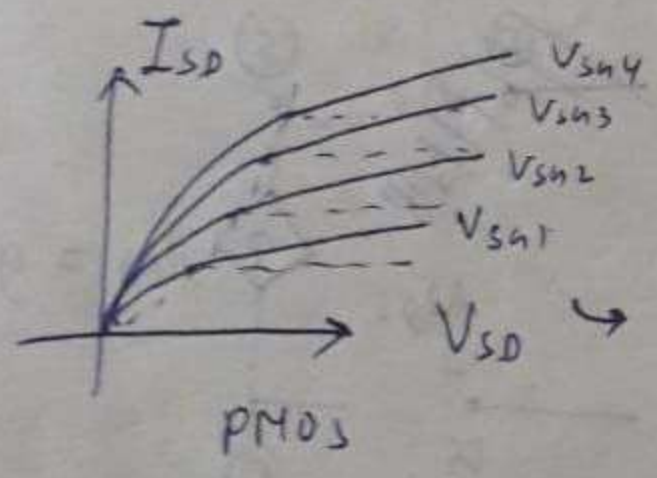

$$I_{SD} = \frac{k_p'}{2}\frac{W}{L}(V_{SG} - |V_{th}|)^2(1 + \lambda V_{SD}) \quad [\text{Saturation}]$$

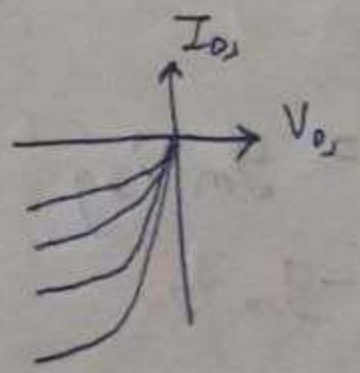


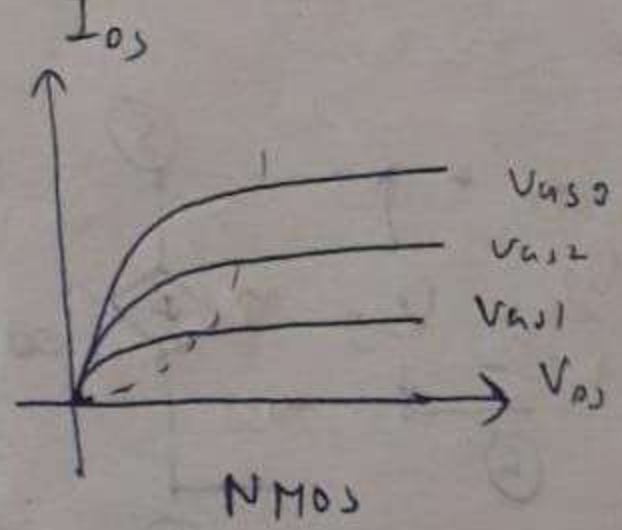

$\Rightarrow$




Small signal → Same as nmos



PMOS

$I_{DS}$ (-ve)

$V_{GS}$ (-ve)

$V_{DS}$ (-ve)

$V_{th}$ (-ve)

→ NMOS type

$I_{SD}$ (+ve)

$V_{SG}$ (+ve)

$V_{SD}$ (+ve)

$V_{th}$ (+ve)

$$|I_{DS}| = \frac{K_p'}{2}\frac{W}{L}\{|V_{GS}| - |V_{th}|\}^2 (1+\lambda|V_{DS}|)$$

For PMOS on:

$$V_{SG} \geq |V_{th}|$$

Triode:

$$V_{DG} > |V_{th}|$$

(No pinchoff)

$V_o$ → Less negative

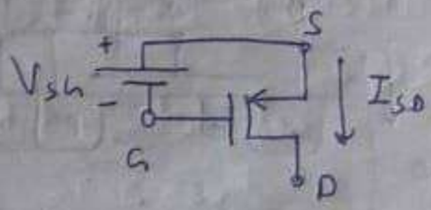
↳ No chance of pinchoff.

Saturation:

$$V_{SD} \geq V_{SG} - |V_{th}|$$

$$\Rightarrow V_{DG} \leq |V_{th}|$$

PMOS: Source is at high potential

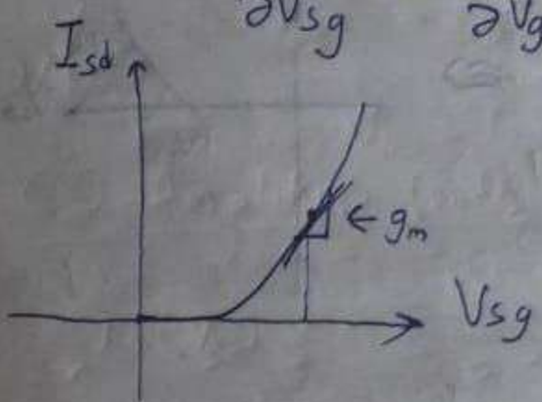


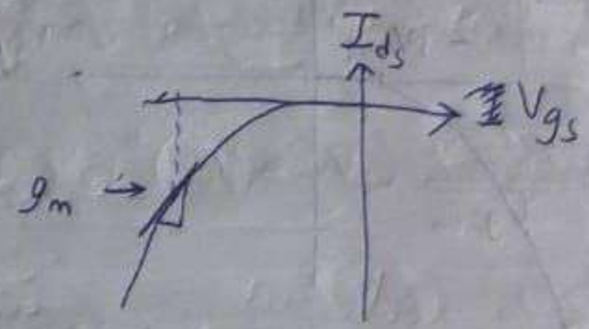

## Small Signal Characteristic Equations and Eq. Ckt:-

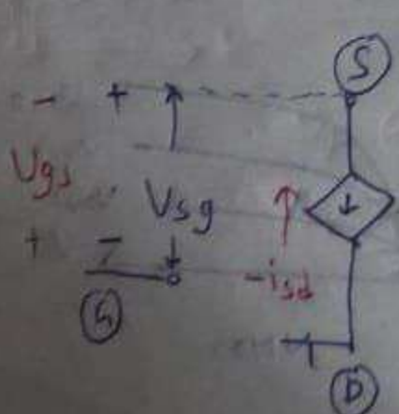
$$i_{sd} = g_m v_{sg} \Rightarrow i_{ds} = g_m v_{gs}$$

[Thus we have same ckt. for PMOS as NMOS]

$$g_m = \frac{\partial I_{sd}}{\partial V_{sg}} = \frac{\partial I_{ds}}{\partial V_{gs}}$$

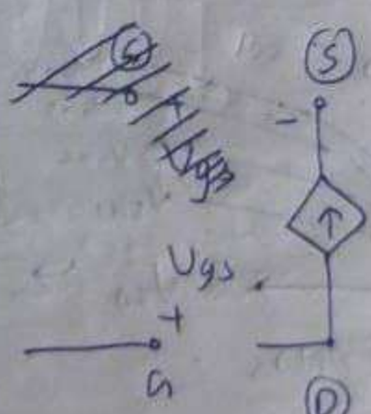



$$i_{sd} = g_m v_{sg}$$

$$= -g_m v_{gs}$$

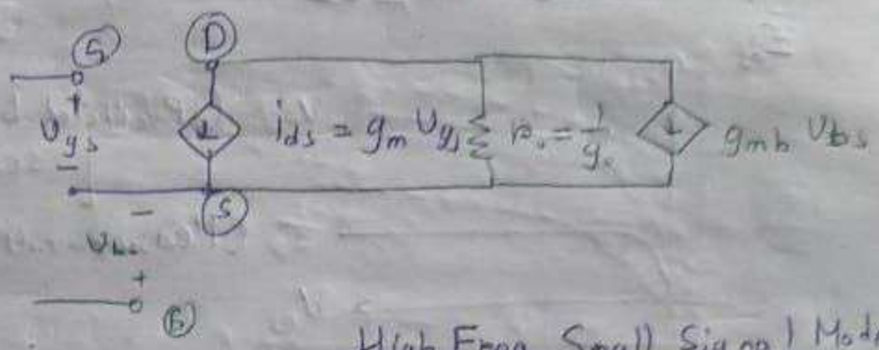



$$i_{ds} = g_m v_{gs}$$

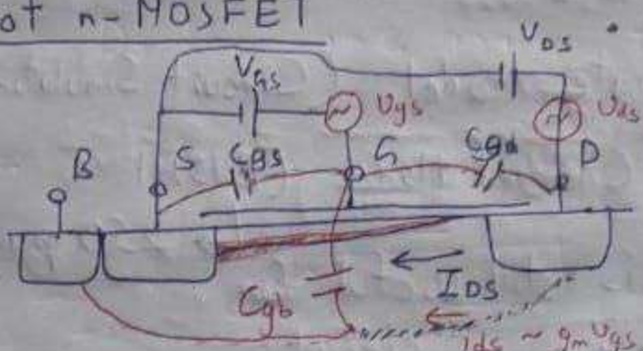
S → DC voltage (ac gnd)

↓ Flip ckt. for convenience

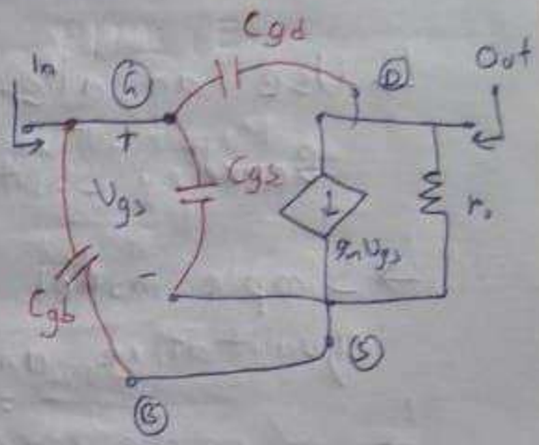
$g_o = \frac{\partial I_{sd}}{\partial V_{sd}} = \frac{\partial I_{ds}}{\partial V_{ds}}$




## Model of n-MOSFET




## High Freq. Small Signal Model




$C_G = C_{ox} WL$ [Cap. at gate]

$C_{gs} = \frac{2}{3} C_G$ [Channel is controlled more towards source side than drain side → U. equal distribution]

$= \frac{2}{3} (C_{ox} WL + C_{ov} W)$ (sat.)

$C_{gd} \simeq 0 + (C_{ov} W)$ (sat.)

$C_{gb} \simeq 0$ [Channel shields gate and body when on]

Fringe effects → $C_{ov}$ ● [Overlap cap.]

↳ Cap / m

Dominant term ← $C_{gs} = \frac{2}{3} C_{ox} WL + C_{ov} W$

Small but careful ← $C_{gd} = C_{ov} W$

$C_{gb} = 0$ (OFF)

$= C_{ox} WL$ (OFF)

$C_{sb}, C_{db}$ → Can be ignored

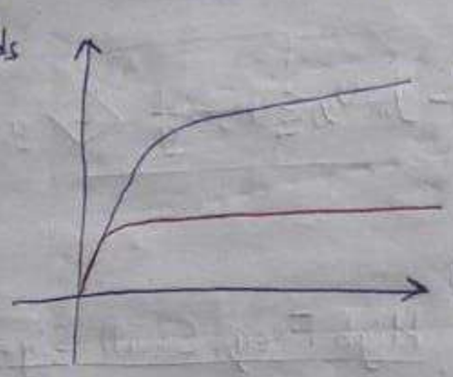
$C_{db}$ → Loads only o/p port

* i/p port loading is dangerous

PMOS → same as NMOS

## Usability of simple model in sub-micron technology

↳ Simple model may be off by a large factor.




↳ Use an alternate model (Circuit Simulators)

Berkeley Short Channel Model (BISM)

↳ > 50 parameters

↳ Simple model is still useful for qualitative analysis of circuit.

↳ $\propto$ power model

$$I_{ds} = \left(\frac{K_n'}{2}\right)\frac{W}{L}(V_{GS}-V_{th})^{\alpha}(1+\lambda V_{ds})$$

↳ Variable fitting and matching with data

$\frac{K_n'}{2} \neq \frac{\mu_n \epsilon_{ox}}{t_{ox}}$

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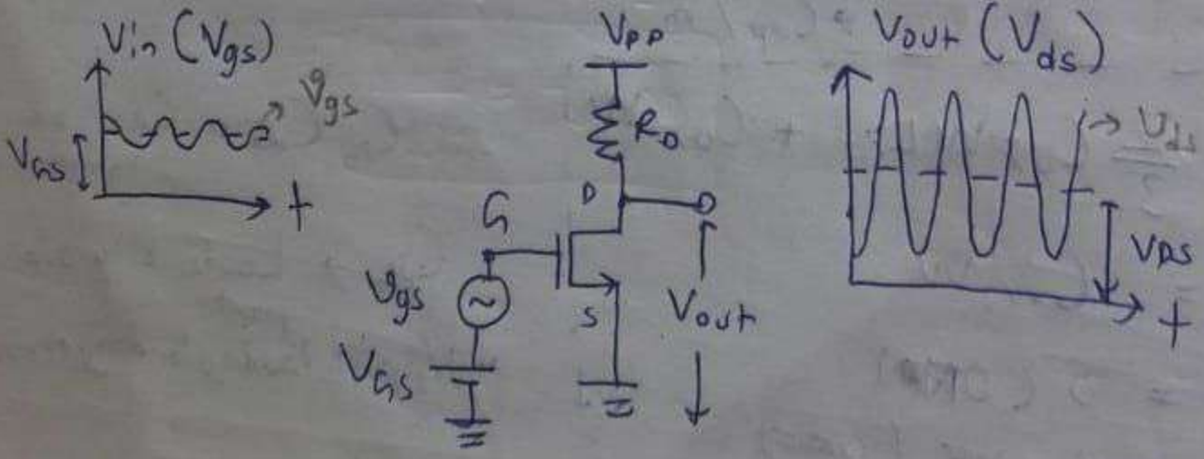
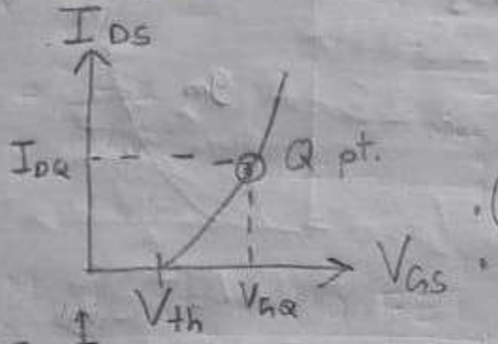
## CS Amplifier (with resistor load)



Biasing → Adjusting DC voltage at i/p ($V_{GS}$) to get a desired small signal characteristic and output DC voltage ($V_{DS}$)

MOS has to remain in saturation. Biasing and resistor values are chosen accordingly.



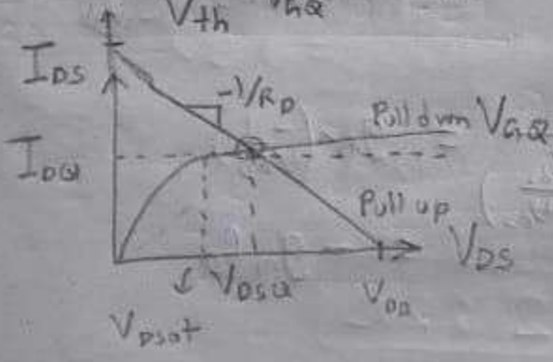

$$I_{DS} = \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{th})^2 (1+\lambda V_{DS})$$
$$\approx I_{DSQ}$$

- $(\frac{W}{L})$ given
- saturation

Pull-up (Load line)

↳ $V_{OUT} = V_{DD} - I_D R_D$

or $I_{DS} = \frac{1}{R_D}(V_{DD} - V_{DS})$




→ Characteristic of pull down element MOSFET (pulls down $V_{out}$ to 0)

$R_D$ → Pull-up [Pulls up $V_{out}$ to $V_{DD}$]

Condition to keep transistor in saturation region:

$V_{DS} > (V_{GS} - V_{th})$ (Assuming $\lambda = 0$)

$\Rightarrow V_{DD} - R_D I_D > V_{GS} - V_{th}$

$\Rightarrow V_{DD} - R_D \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{th})^2 > (V_{GS}-V_{th})$

Find max. value of $R_D$ if all parameters are known :-

$R_D \cdot \frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{th})^2 < V_{DD} - (V_{GS}-V_{th})$ $\quad V_{DSat} = V_{GS} - V_{th}$

$R_D < \dfrac{V_{DD} - (V_{GS}-V_{th})}{\frac{K_n'}{2}\frac{W}{L}(V_{GS}-V_{th})^2} = R_{Dmax}$ We take $R_D = \frac{R_{D\_max}}{2}$ [For more signal headroom]

Find value of $V_{GS}$, if $R_D$ is known: $\quad R_{D\_max} = \dfrac{V_{DD}-V_{dsat}}{I_D}$

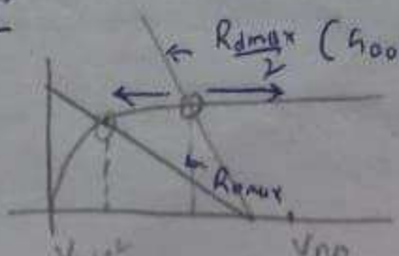
Let $V_{GS} - V_{th} = x$

Solve: $V_{DD} - R_D \frac{K_n'}{2}\frac{W}{L}x^2 = x$ → Solve quadratic

$R_D \frac{K_n'}{2}\frac{W}{L}$

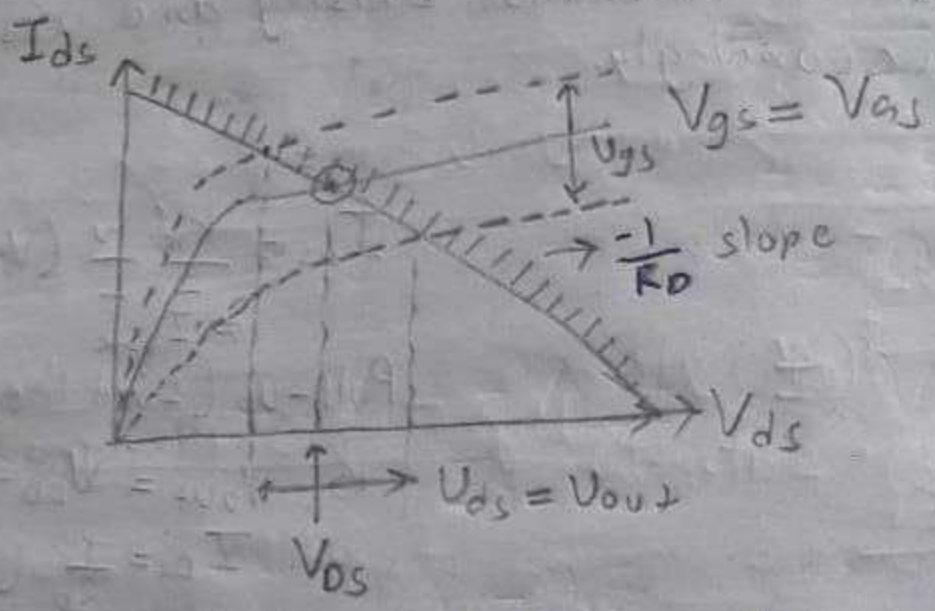
If $R_D = R_{Dmax}$

↳ Edge of saturation



Instantaneous signal Analysis

$$I_{ds} = I_{DS} + i_{ds} = \frac{K_n'}{2}\frac{W}{L}(V_{GS} + v_{gs} - V_{th})^2 (1 + \underbrace{\lambda(V_{DS} + v_{ds})}_{\approx 1})$$



$$\text{Magnification} = \frac{\partial I_{ds}}{\partial V_{gs}} \times \frac{1}{\left(\frac{\partial I_{ds}}{\partial V_{ds}}\right)} = g_m \times \left(\frac{-1}{\frac{1}{R_D}}\right)$$

$$\left(\frac{\partial V_{ds}}{\partial v_{gs}}\right) = -g_m R_D$$

$$\therefore \boxed{\frac{v_{out}}{v_{gs}} = -g_m R_D}$$

$$V_{OUT} = V_{DD} - R_D \frac{K_n'}{2}\frac{W}{L}(V_{GS} - V_{th})^2 \left[1 + \frac{v_{gs}}{(V_{GS} - V_{TH})}\right]^2$$

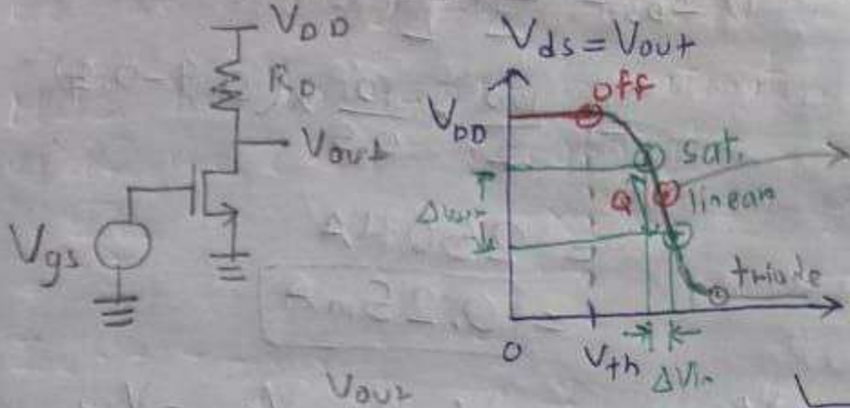
↓ Linearised expression

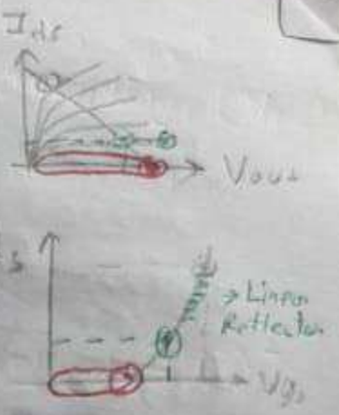
$$V_{out} = \underbrace{V_{DD} - R_D I_{DS}}_{V_{DS} = V_{out}} - \underbrace{R_D K_n' \frac{W}{L}(V_{GS} - V_{TH}) v_{gs}}_{R_D g_m v_{gs} = v_{out}}$$

$$v_{out} = -g_m R_D v_{gs}$$

$$\therefore \boxed{\frac{v_{out}}{v_{gs}} = -g_m R_D}$$

# Linearization / Small signal equivalent circuit



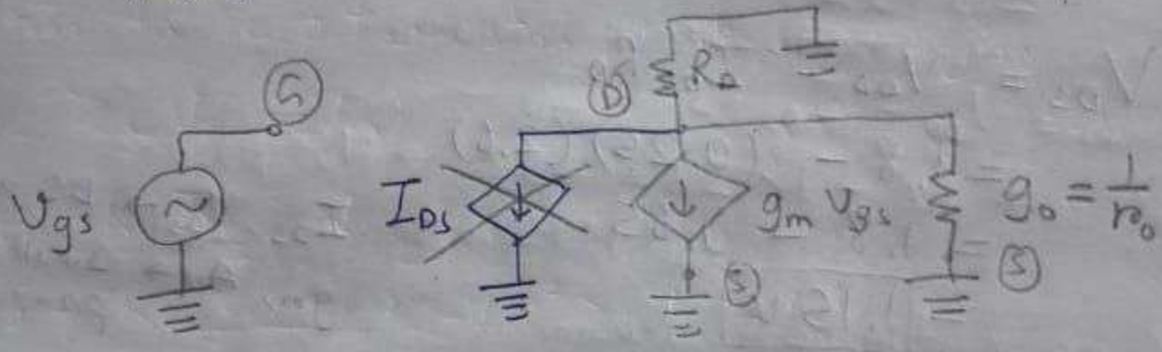




↳ Superposition theorem can't be applied here.

Translation about Q-point → Aligning all DCs=0 [Linear characteristic]

Small signal analysis [All DC=0] ↳ Translation of axes

↳ Superposition theorem can be applied here (passes through origin)




Find Q-point, find small signal parameters and then forget it.

[Solve the numerical - Saturday]

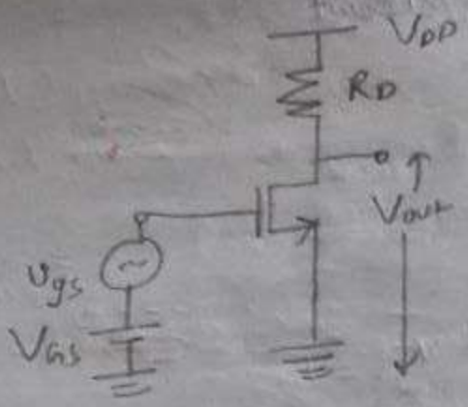
***

12/9/20 **Numerical-1**

Given: 1) $K_n' = 100 \mu A/V^2$ 2) $V_{th} = 0.4V$ 3) $W = 10 \mu m$
4) $L = 0.5 \mu m$ 6) $V_{DD} = 1.8V$ 7) $V_{GS} = 0.9V$
8) $R_D = 0.5 R_D(max)$ 9) $\lambda \approx 0$

Sequence of calculation:

i) $I_{DS}$ ii) $R_D$ iii) $V_{DS}$ iv) $g_m$ v) $A_v$




i) $I_{DS} = \frac{K_n'}{2}\frac{W}{L}(V_{GS} - V_{th})^2$

$= \frac{100}{2} \times \frac{10}{0.5} \times (0.9 - 0.4)^2$

$= 250\,\mu A$

$= \boxed{0.25\,mA}$

ii) $R_{D(max)} = \frac{V_{DD} - V_{osat}}{I_{DS}}$

$V_{osat} = V_{GS} - V_{tH}$

$= 0.9 - 0.4$

$= 0.5V$

$= \frac{1.8 - 0.5}{0.25}$

$= 5.2\,k\Omega$

$\therefore R_D = \frac{1}{2}(5.2\,k\Omega) = \boxed{2.6\,k\Omega}$

iii) $V_{DS} = V_{DD} - I_{DS} R_D$

$= 1.8 - (0.25)(2.6)$

$= 1.8 - 0.65$

$= \boxed{1.15\,V}$

$I_{DS}, V_{DS}$ → DC parameters

$g_m, A_v$ → Small signal parameters

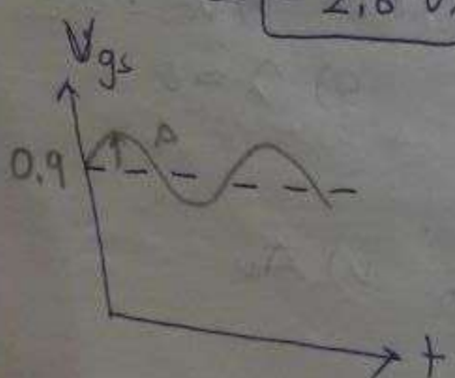
iv) $g_m = K_n' \frac{W}{L}(V_{GS} - V_{th})$

$= (0.1) \times \frac{10}{0.5} \times (0.9 - 0.4)$

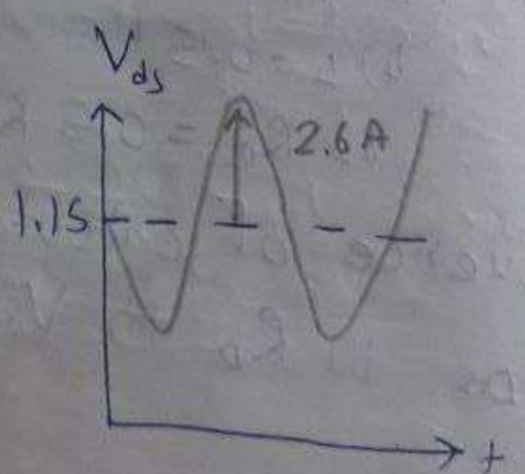
$= \boxed{1\,mA/V}$

v) $A_v = -g_m R_D = (-1\,mA/V \times 2.6\,k\Omega)$

$= \boxed{-2.6\,V/V}$



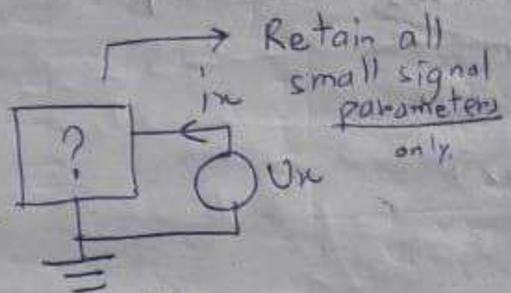

Very less gain



We have to modify circuit parameters to get good gain.

NOTE: $A_V = \frac{v_{out}}{v_{in}}$ ⟶ Small signal (ac only)

Node impedance:




↓

All independent sources are removed because they may interfere with $V_x$.

$r_x = \frac{V_x}{i_x}$

Numerical-2 (Same circuit)

Rest other parameters same

Given: $W = 40\,\mu m$ (changed) $10 \rightarrow 40$

$V_{GS} = 0.65\,V$ ($0.9 \rightarrow 0.65$)

$V_{th} = 0.4\,V$ (Same)

$$I_{DS} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_{th})^2$$

$I_{DS}$ remains constant

$W \uparrow (4\times)$ $(V_{GS} - V_{th}) \downarrow (\frac{1}{2}\times)$

i) $I_{DS} = \underline{0.25\,mA}$ (same)

ii) $V_{DS} = \underline{1.15\,V}$ (same)

iii) $g_m = k_n' \frac{W}{L}(V_{GS} - V_{th})$

$\frac{W}{L} \uparrow (4\times)$

$(V_{GS} - V_{th}) \downarrow (\frac{1}{2}\times)$

$\therefore g_m \uparrow (2\times)$

$\Rightarrow g_m = 2 \times 1 = \underline{2\,mA/V}$ (doubles compared to earlier example)

iv) $A_V = -g_m R_D$

$= \underline{-5.2\,V/V}$ (Gain doubles)

Check: $L \nearrow (4\times)\uparrow \rightarrow (V_{GS} - V_{th})$ same as 1 $\rightarrow$ Gain remains constant.

$I_{DS}$ const.

$C_G \uparrow (16\times)$

But $A = W \times L \rightarrow$ (channel) area becomes 16 times higher

∴ $C_{gs}$ goes up 16 times. $\left[\frac{2}{3} C_{ox} WL\right]$

Increasing W, L by same amount keeps other properties same but increases load cap. and has poor freq. response.

**Numerical -3** (Same ex.)

$W = 40\,\mu m$

$L = 0.5\,\mu m$

$V_{GS} = 0.9V$ (Same as 1)

$(V_{GS} - V_{th})$ constant → $I_{DS}$ changes

$$I_{DS} = \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \quad (W \uparrow 4x)$$

$$= 4 \times 0.25\ mA$$

$$= \underline{1\,mA}$$

$$V_{DS} = V_{DD} - I_{DS} R_D$$

$$= 1.8 - 1 \times 2.6 = -0.8 \rightarrow \text{Not possible}$$

∴ MOS in triode

∴ Check for new $R_{D\_max}$:

$$R_{D\_max} = \frac{V_{DD} - V_{dsat}}{I_{DS}} = \frac{1.8 - 0.5}{1} = \underline{1.3\,k\Omega}$$

$$\Rightarrow R_D = \frac{1}{2} \times 1.3 = \underline{0.65\,k\Omega} \rightarrow V_{DS} = \underline{1.15V}$$

$$g_m = \sqrt{2 k_n' \frac{W}{L} I_{DS}} = k_n' \frac{W}{L} (V_{GS} - V_{th}) \quad (4x)\uparrow$$

$$= 4 \times \text{original}$$

$$= 4 \times 1$$

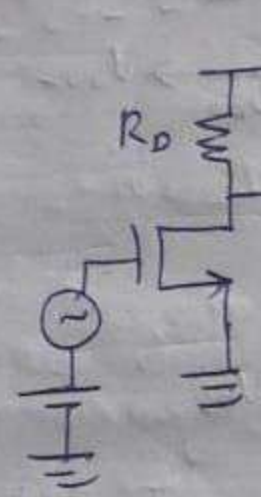
$$= \underline{4\ mA/V}$$

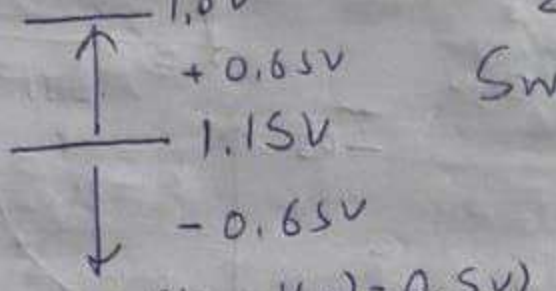
$$A_V = -g_m R_D = -4 \times 0.65 = \underline{-2.6\,V/V}$$

∴ Simply increasing $\left(\frac{W}{L}\right)$ keeping $V_{GS}$ constant doesn't change voltage gain as $R_D$ has to be lowered.

However $R_D$ is low ⇒ Lower loading effect (Advantage)
[Will come soon]

Refer Chart in Slides [Comparision and Conclusion]




$\Delta V_{out}$

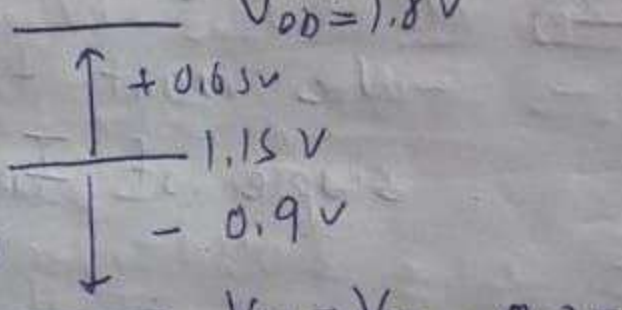
Swing o/p: $2 \times 0.65 = 1.3V$

$$C_{gs} = \frac{2}{3} C_{ox} WL$$

$$= \frac{2}{3} \times 10 \times 10 \times 0.5 = \frac{100}{3} fF$$

$R_{out} = R_D = 2.6k\Omega$

2nd case




$0.65 + 0.9 = 1.55V$

$\therefore$

W ↑ $V_{GS}$ ↓ ⇒ Swing ↑, $A_v$ ↑ (Good)
$C_{in}$ ↑ (Bad)

$P_{diss} = V_{DD} \times I_{DS}$

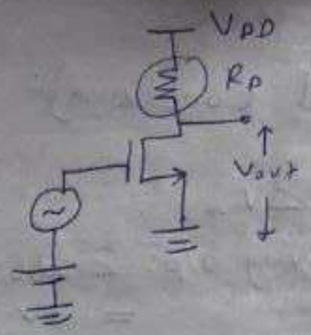
Do yourself: 1) $\frac{W}{L}(M\times)\uparrow\downarrow$, $(V_{GS} - V_{TH})(N\times)\uparrow\downarrow$

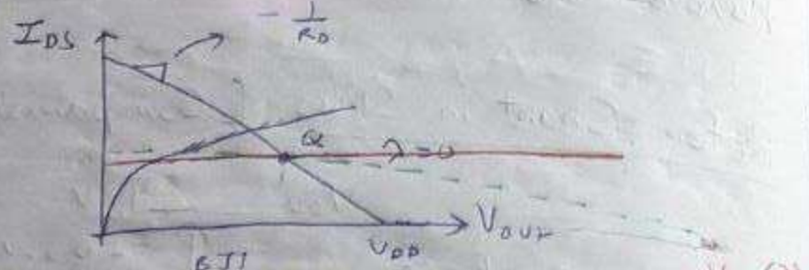
~~$I_{DS}$ (Constant)~~ → Find changes

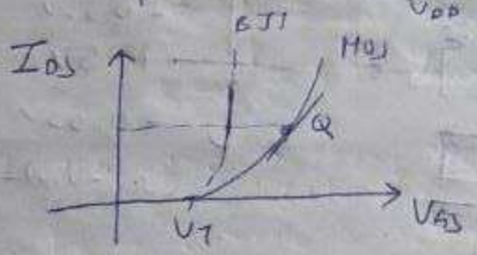
2) $\left(\frac{W}{L}\right)(M\times)\uparrow\downarrow$, $I_{DS}(P\times)\uparrow\downarrow$

↳ Find changes

# Common Source Amplifier (with active load)




$|A_v| = g_m R_D$

↓

Slope of $I_{DS} - V_{GS}$ × $\frac{1}{\text{Slope of } I_{DS} - V_{out}}$

$g_{m\_BJT} = \frac{I_C}{V_T} >> g_{m\_MOS}$

We can't use BJT [So $g_m$ can't be improved]

If $R_D \uparrow$ (—), same $g_m \Rightarrow |A_v| \uparrow$

We want to lower slope of $I_{DS} - V_{out}$.

↓

Keep same Q-pt.

↳ Decrease $I_{DS} - V_{out}$ slope.

⇓

Increase $R_D \uparrow$ => Corresponding $V_{DD}$ (?) very high

↓

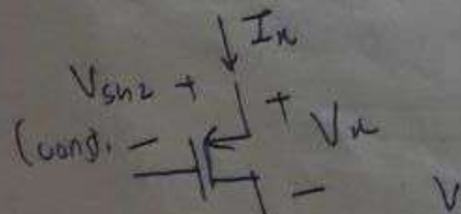
Not possible in CMOS technology

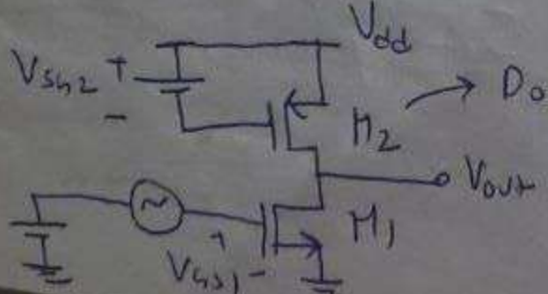
Can we have some characteristic like this?

$\frac{\partial i_d}{\partial v_{out}} \uparrow\uparrow$ and it is limited to $V_{dd}$

⇓

We are looking for active device.

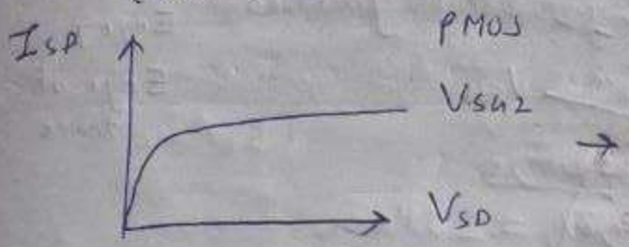



$V_{gs1}, V_{sh2} \rightarrow M_1, M_2$ in saturation

→ Does it give some characteristic

We see $I_x - V_x$ char. for given $V_{sg2}$.
($I_{SD}$) ($V_{SD2}$)



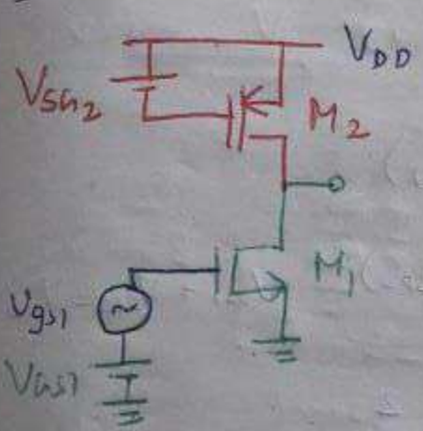

→ Thus we get the required characteristic.

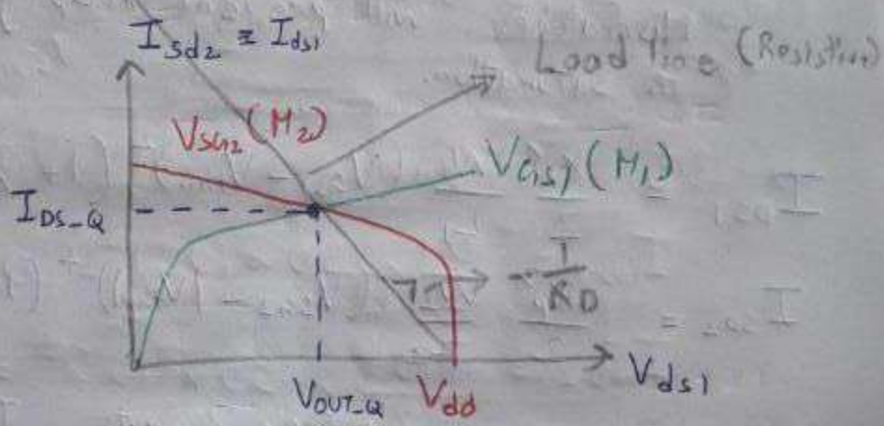
(?)

14/9/20 (Week-3)

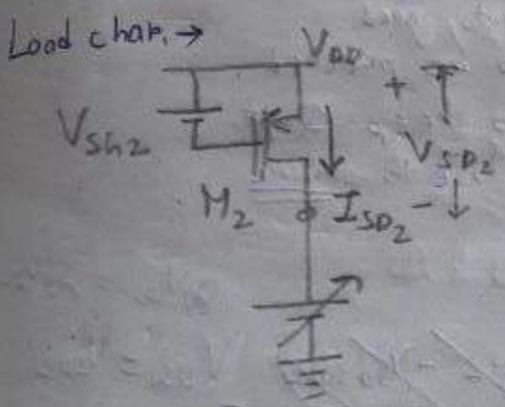
## CS amplifier with active load (current source load)

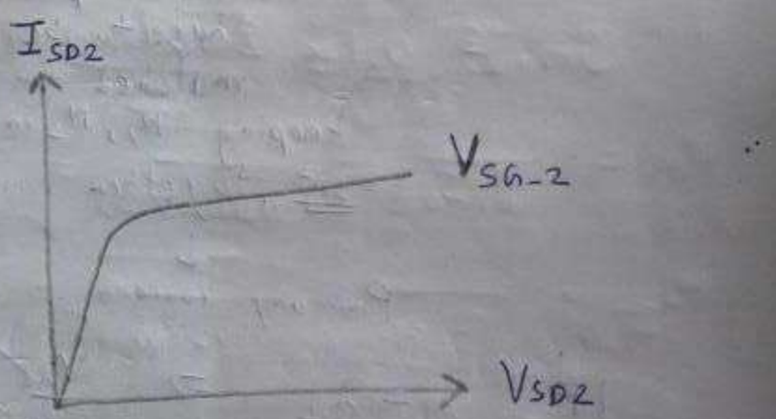
### Basic config. and Biasing




Load char. →




How to get red $V_{sg2}(M_2)$ characteristics

⇓

1st graph: x-axis ≡ $V_{ds1}$ ⇐ See axis

2nd graph: x-axis ≡ $V_{sd2}$

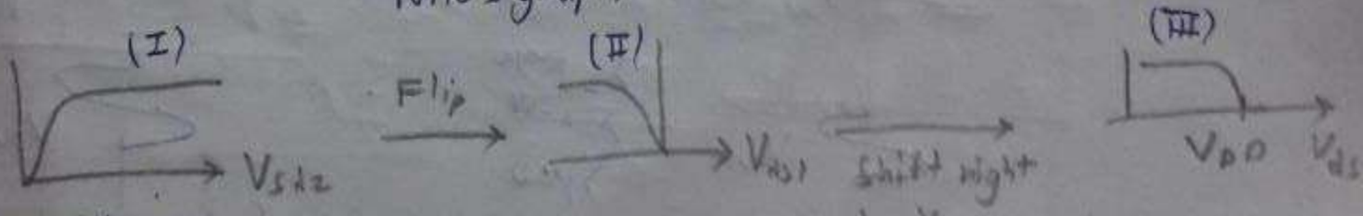
y-axis: $I_{sd2} = I_{ds1}$

⇒ Now $V_{SD2} + V_{DS1} = V_{DD}$ [KVL]

⇒ $V_{DS1} = V_{DD} - V_{SD2}$ → Flip and shift right by $V_{DD}$

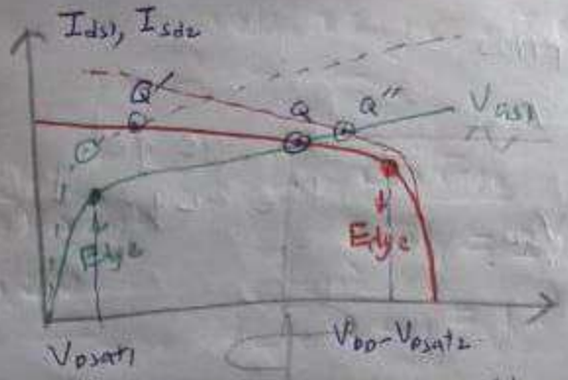
↓

Translation of PMOS characteristic to NMOS graph




3 step process

# Condition to keep transistors in saturation region:




Edge 1
Edge of triode

If Edge current levels are same → then we get same saturation for both devices
(However Q being in middle is not guaranteed)

Mismatches will prevent keeping both transistors in saturation.

$$I_{DS1} = \frac{K_n'}{2}\frac{W_1}{L_1}(V_{GS1} - V_{thn})^2(1+\lambda_1 V_{DS1})$$

$$I_{SD2} = \frac{K_p'}{2}\frac{W_2}{L_2}(V_{SG2} - |V_{thp}|)^2(1+\lambda_2 V_{SD2})$$

$V_{DS1} + V_{SD2} = V_{DD}$

↳ These 2 parts have to be matched for keeping $M_1, M_2$ in sat. together → Primary concern

These 2 parts need to be matched to keep Q-pt. close to middle

$\lambda_1 V_{DS1} = \lambda_2 V_{SD2}$

IF $\lambda_1 = \lambda_2 \Rightarrow V_{DS1} = V_{SD2}$

$$\frac{V_{dd}}{2} + \frac{(V_{DSatn} - V_{SDsatp})}{2} = V_{out}$$

$$V_{out} \approx \frac{V_{dd}}{2}$$

$V_{gs1}$ change → Shifts pull down chan. → Q pt (Inst.) changes → AC variation in o/p signal

$\lambda \to 0 \Rightarrow$ small $v_{gs1} \Rightarrow$ large $V_{out}$ swing

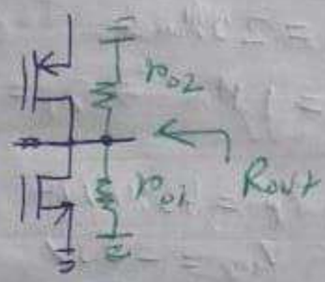
$\lambda_2$ large
$\lambda_1$ small
$\lambda_1 \approx 0$
$\lambda_2 \gg 0$

$\lambda_1 \approx \lambda_2 \approx 0$

(Higher gain)

Smaller $\lambda$s → Higher gain
↳ Large $V_{out}$ swing /gain

∴ To increase swing ^ we must decrease $\lambda$s i.e. improve / increase $r_{o1}$, $r_{o2}$.



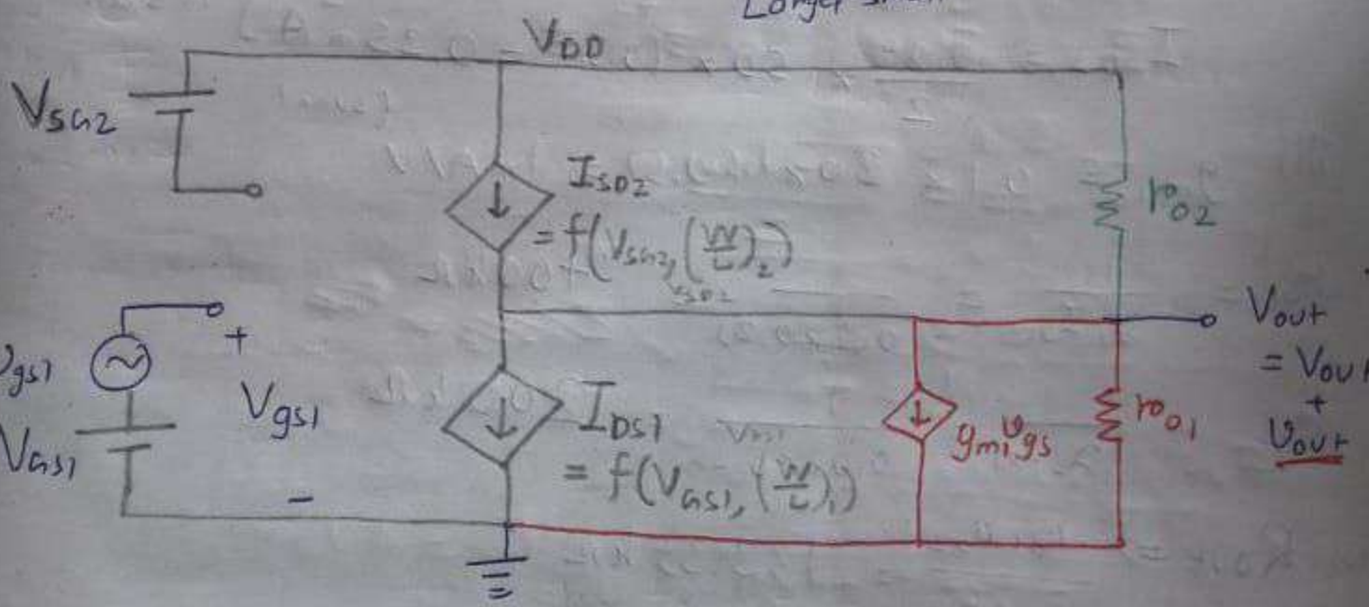

$R_{out} = r_{o1} || r_{o2}$

$r_o = \frac{1}{\lambda I_o}$

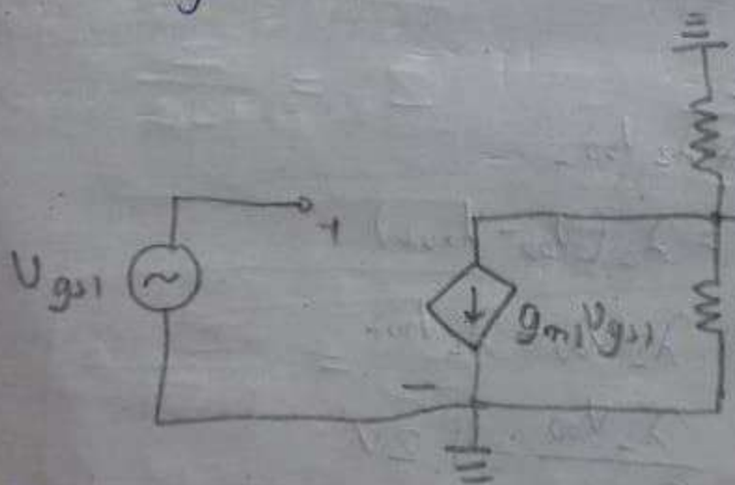
∴ Without changing $g_m$ we have improved gain because of smaller slope of $I_{DS}$ - $V_{out}$ because of active device char.

## Small Signal equivalent circuit

Longer Small




## Suppressing DC information:-




$I_{DS1} = I_{SD2}$

$\lambda V_{DS}$ → ignored

↓

If not equal excess current flows through $r_{o1}$ or $r_{o2}$ ↓

Forces either transistor to be in triode

[ $v_{gs1} = 0$, $V_{in}, I_x \rightarrow V_{out}$ ]

$A_V = \frac{v_{out}}{v_{in}} = -g_{m1}(r_{o1} || r_{o2})$

$R_{out} = r_{o1} || r_{o2}$

Assign-2 (Deadline: Tomorrow Midnight) → Wednesday

***

avlsiassignment@gmail.com

15/9/20

Numeric

$K_n' = 100\,\mu A/V^2$

$V_{tn} = 0.4V$

$W_2 = 25\mu m$

$L_2 = 0.5\mu m$

$\lambda_2 = 0.02\,V^{-1}$

Change $(L_1 \neq L_2)$

Both changed: $W_1 = 20\mu m$, $L_1 = 1\mu m \rightarrow \lambda_1 = \frac{0.01}{1} = 0.01\,V^{-1}$

$K_p' = 40\,\mu A/V^2$

$V_{tnp} = -0.3V$

$V_{dd} = 1.8V$

$V_{GS1} = 0.9V$ $V_{SG2} = 0.8V$

i) Dominant part:

$I_{DS1} = \frac{0.1}{2} \times 20 \times (0.5)^2 = 0.25\,mA$

$I_{SD2} = \frac{0.04}{2} \times 50 \times (0.5)^2 = 0.25\,mA$ (same)

} Both one in sat.

iii) $g_{m1} = 0.1 \times 20 \times (0.5) = 1mA/V$

$r_{o1} = \frac{1}{\lambda_1 I_{DS}} = \frac{1}{0.01 \times 0.25} = 400k\Omega$

$r_{o2} = \frac{1}{\lambda_2 I_{DS}} = \frac{1}{0.02 \times 0.25} = 200k\Omega$

iv) $R_{out} \Rightarrow \frac{r_{o1} r_{o2}}{r_{o1} + r_{o2}} = 133.33\,k\Omega$

v) $|A_v| = g_m R_{out} = 1mA/V \times 133.33 = 13333\ V/V$

$I_{DS1} = I_{SD2}$

$\Rightarrow \lambda_1 V_{DS1} = \lambda_2 V_{SD2}$

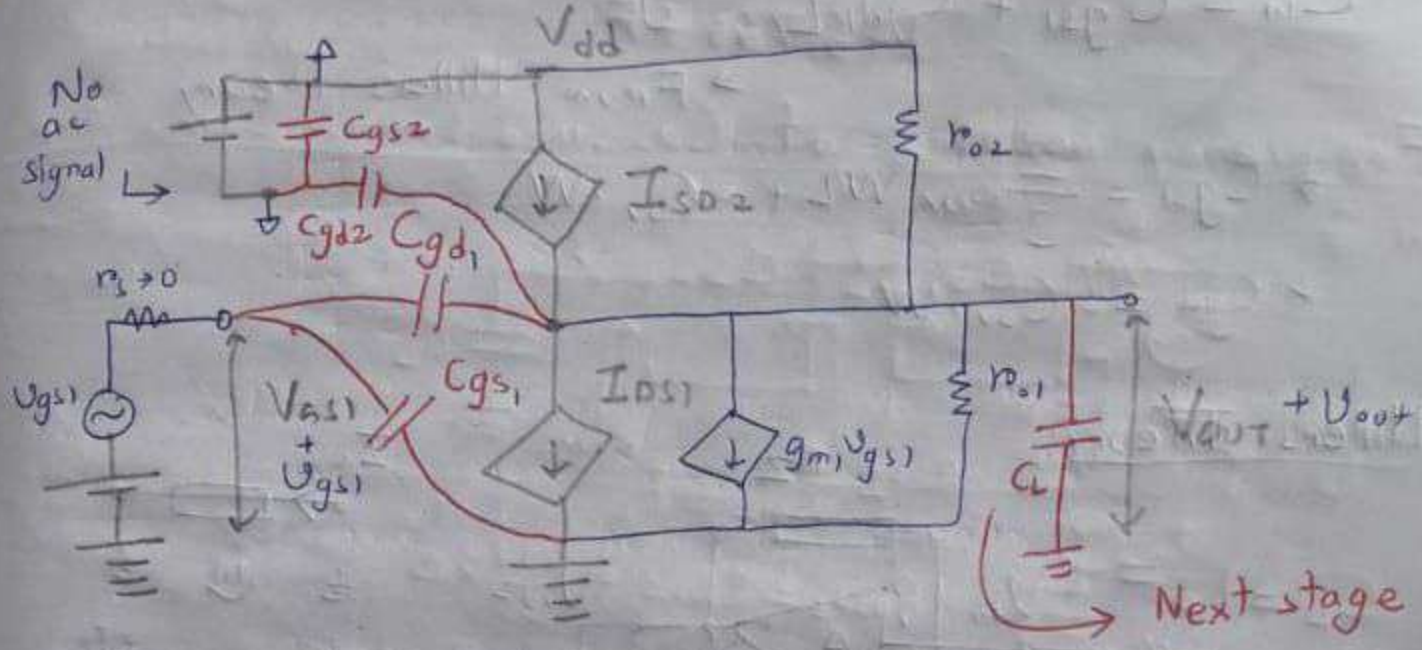
$\Rightarrow \lambda_1 (V_{out}) = \lambda_2 (V_{DD} - V_{out})$

$\Rightarrow \lambda_1 V_{out} = \lambda_2 V_{DD} - \lambda_2 V_{out}$

$\Rightarrow V_{out} = \frac{\lambda_2 V_{DD}}{\lambda_1 + \lambda_2} = 1.2V$

# Frequency Response

HF small signal eq. circuit

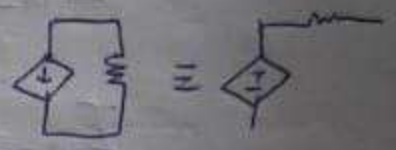



$C_{gs2}$ b/w 2 ac gnd → no role to play

$C_{gs1}$, $C_{gd1}$ → Signal i/p loading

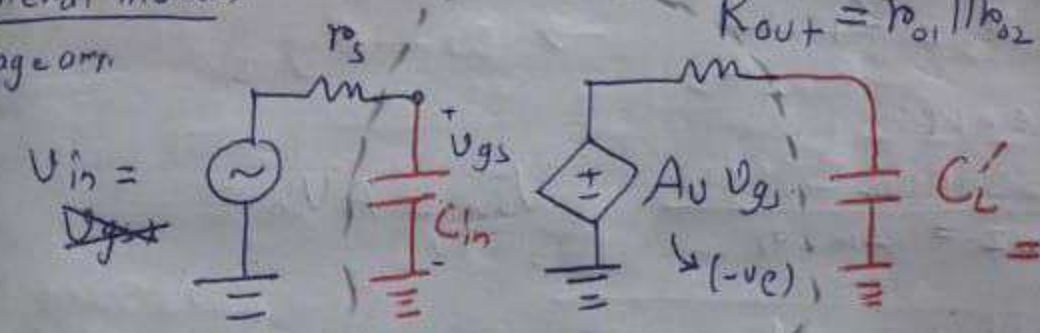
$C_{gd1}$, $C_{gd2}$ → o/p port loading

small signal only!

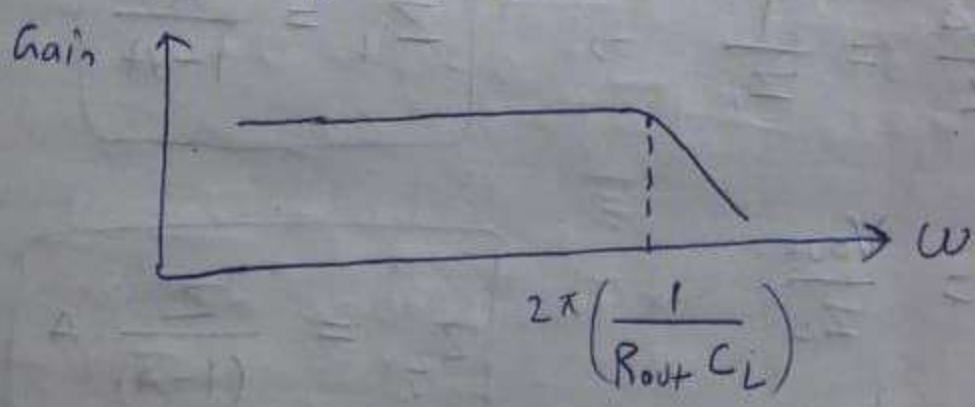


General model →

(Voltage amp.)




$A_V$ → mid-frequency gain




Bandwidth:

$BW_1 = \frac{1}{r_s C_{in}}$ ;

$BW_2 = \frac{1}{R_{out} C_L}$ ;

$BW_{3\text{-}dB} = \min(BW_1, BW_2)$

Next task → How to improve Bandwidth?

$r_s$, $C_L$ → given to us

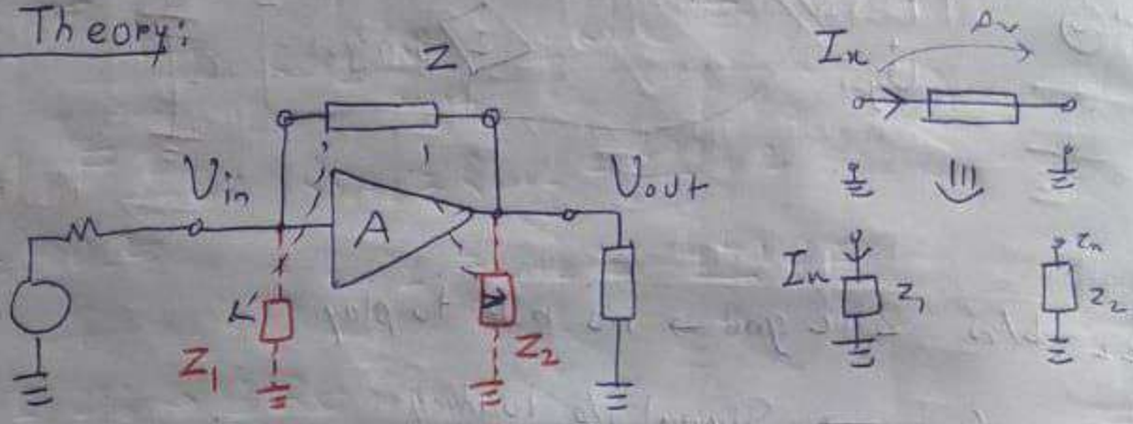
Our effort ⇒ $R_{out}$, $C_{in}$ minimisation

$$C_{in} = C_{gs1} + C_{gd1}\,[\ ,\ ]$$

↳ From Miller's Theory

* $C_{gs1} = \frac{2}{3} C_{ox} WL + C_{ov} \cdot W$
* $C_{gd} = C_{ov} \cdot W$

Miller's Theory:




$$I_{in-Z} = \frac{V_{in} - V_{out}}{Z}$$

$$I_{in-Z_1} = \frac{V_{in}}{Z_1}$$

For equivalence

$$I_{in-Z} = I_{in-Z_1} \qquad V_{out} = A V_{in}$$

$$\Rightarrow \frac{V_{in} - V_{out}}{Z} = \frac{V_{in}}{Z_1}$$

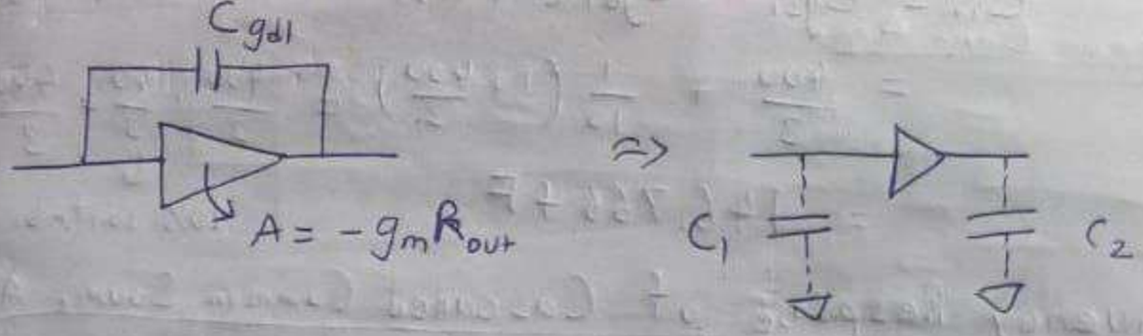
$$\Rightarrow \frac{1-A}{Z} = \frac{1}{Z_1} \Rightarrow \boxed{Z_1 = \frac{Z}{1-A}}$$

$$\frac{V_{in} - V_{out}}{Z} = \frac{V_{out}}{Z_2}$$

$$\frac{\left(\frac{1}{A} - 1\right)}{Z} = \frac{1}{Z_2}$$

$$\boxed{Z_2 = \frac{Z}{(1-A)} \cdot A}$$

Application in finding $C_{in}$:




$$C_1 = C_{gd}(1-(-g_m R_{out}))$$

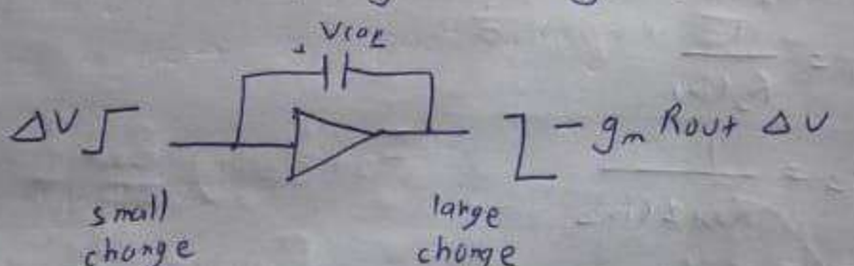
$$= C_{gd}\underbrace{(1+g_m R_{out})}$$

Correction factor mentioned earlier

This technique is possible only in mid-freq where $V_{out} = A_v V_{in}$ only holds ~~valid~~ valid. → Not applicable at HF

$$C_2 = C_{gd}\left(1+\frac{1}{g_m R_{out}}\right) \approx C_{gd}$$

Due to Miller effect, $C_{gd}$ has big impact on i/p side.




$$V_{cap} = (1+g_m R_{out})\Delta V \rightarrow Q_{drawn} = C(1+g_m R_{out})\Delta V$$

Actually amount of charge drawn is very high.

$C_{eff}$ from i/p side → $\frac{Q_{drawn}}{\Delta V} = C(1+g_m R_{out})$

$A > 0 \rightarrow Z(-ve)$

-ve cap. → may reduce total cap. at some node
↳ not used to replace inductor

Numeric

Some values as today's prev numeric

$C_{ov} = 0.005\ fF/\mu m$

$A_v = -\frac{400}{3}$

$C_{gs1} = \frac{2}{3} C_{ox} W L_1$

$= \frac{2}{3} \times 10 \times 20 \times 1$

$= 133.33\ fF$

↳ 0.1 negligible so no $C_{ov}W$

$C_{gd} = C_{ov} W$

$= 0.1\ fF$

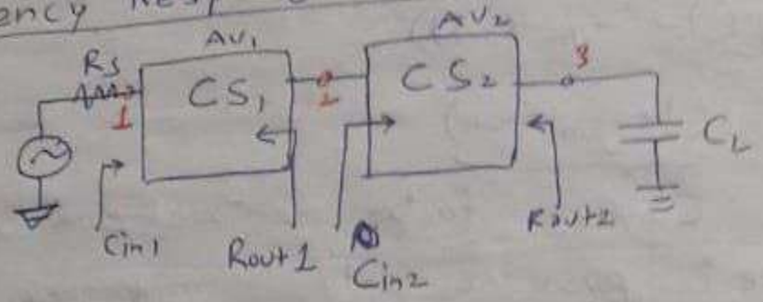
$$C_{in} = C_{gs1} + C_{gd1}(1 + A_v)$$

$$= \frac{400}{3} + \frac{1}{10}\left(1 + \frac{400}{3}\right) = \frac{400}{3} + \frac{40}{3} = \frac{440}{3}$$

$$= 146.766\ fF$$

10% contrib.

## Frequency Response of Cascaded Common Source Amps.




Assuming $R_{in} \to \infty$, $r_{out} \to 0$

$C_L = 1\ pF$ $\qquad R_{out2} = R_{out2} = \frac{400}{3}\ k\Omega$

$R_S = 100\ \Omega$ $\qquad C_{in1} = C_{in2} = \frac{440}{3}\ fF$

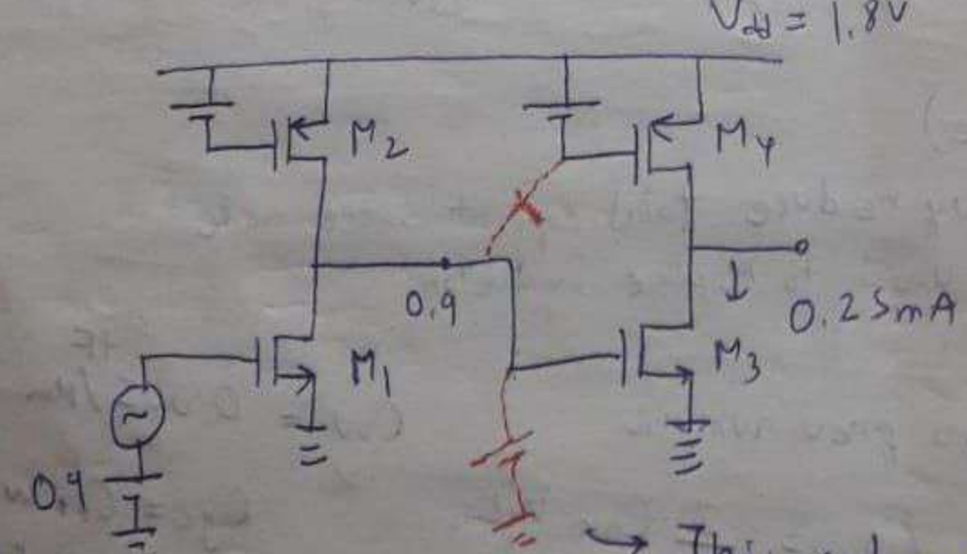
1, 2, 3 → 3 RC nodes

$$BW_1 = \frac{1}{R_S C_{in1}}$$

$$BW_2 = \frac{1}{R_{out1} C_{in2}}$$

$$BW_3 = \frac{1}{R_{out2} C_L} \rightarrow \text{Dominating}$$

## Biasing of Cascaded Stages




We are lucky over here

$V_{out}$ is same as biasing $V_{in}$

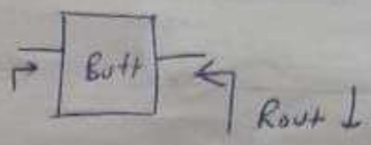
→ This scheme will work.

↳ Some adjustments need to be do

$(V_{SG4} - |V_{thp}|) = 0.6V$

We have to do something at node-3 to improve bandwidth, followed by node 2.

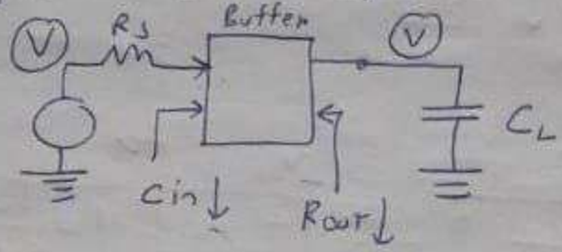
↳ Solution: Put a buffer. →



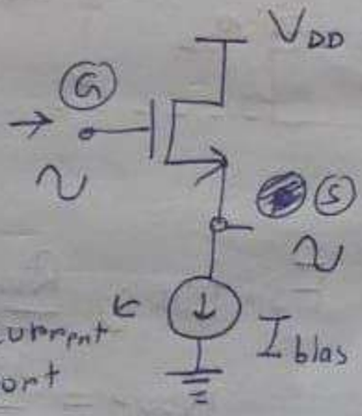

Maybe no voltage gain. But helps $C_{in}$↓ reduce loading effect.

Buffer - Common drain amplifier (Small $R_{out}$, Small $C_{in}$)

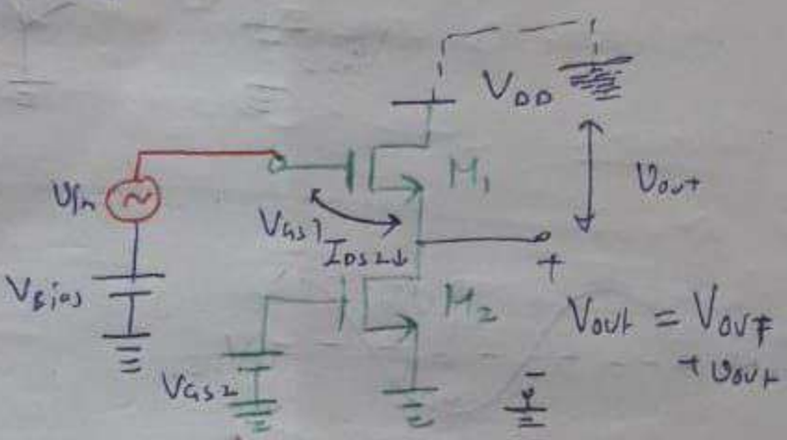
↳ Voltage mode of operation



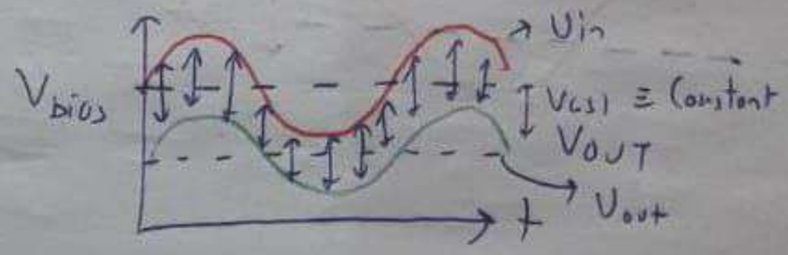

## Config, Biasing and Operation




No amplification
↓
DC voltage shift




$V_{gs1}$ → supports $I_{bias}$




$r_{o2} \to \infty$, $r_{o1} \to \infty$

$I_{DS1} = I_{DS2} = $ Const.

↓

Independent of signal

$R_{out}$ also small

$$C_{in} = C_{gs1}(1 - A) + C_{gd1}$$

$$= 0 + C_{gd1}$$

$= C_{gd1}$ → very small (compared to $C_{S_{amp}}$)

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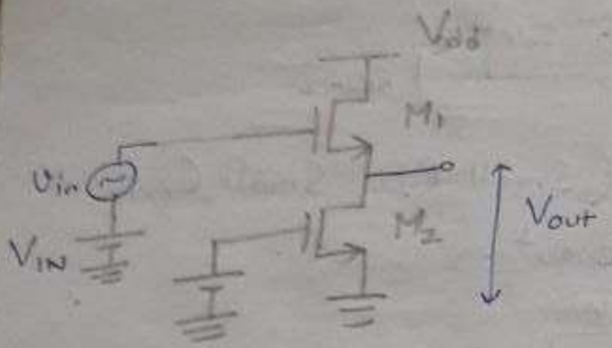
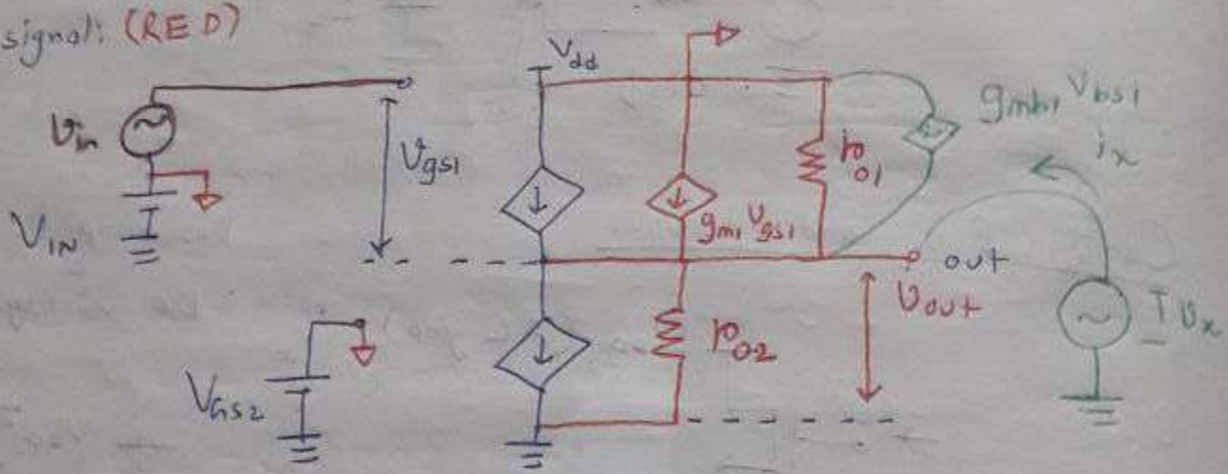
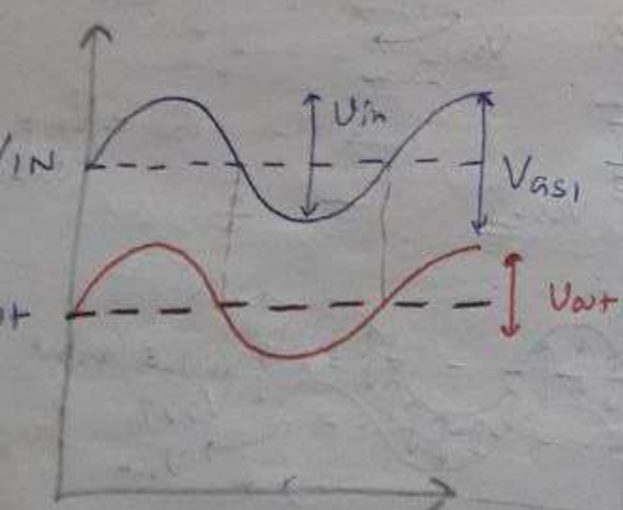
## Common Drain Amp.




Small signal: (RED)

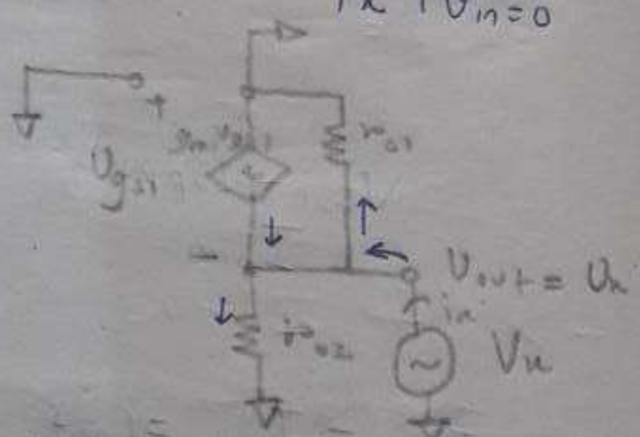



C shifter by $V_{gs1}$ amount
cided by $I_{bias}$.

For finding $R_{out}$ $[v_{in}=0]$ ∴

$$R_{out} = \frac{v_x}{i_x}\Big|_{v_{in}=0}$$




$V_{gs1} = 0 - V_x = -V_x$

KVL at out:

$$i_x = \frac{V_x}{r_{o2}} + \frac{V_x}{r_{o1}} - g_{m1} V_{gs1}$$

$$i_x = V_x\left(\frac{1}{r_{o2}} + \frac{1}{r_{o1}} + g_{m1}\right)$$

$$\therefore R_{out} = \frac{1}{\frac{1}{r_{o1}} + \frac{1}{r_{o2}} + g_{m1}} = r_{o1} \| r_{o2} \| \frac{1}{g_{m1}}$$

Finding $A_v$:

(Refer Big small signal ckt)

$$R_{out} = r_{o1} \| r_{o2} \| \frac{1}{g_{m1}}$$

If Body - Source are not shorted

$$R_{out} = r_{o1} \| r_{o2} \| \frac{1}{g_{m1}} \| \frac{1}{g_{mb1}}$$

↳ $\sim \frac{1}{g_m}$; Small [Handy analysis]

$V_{gs1} = V_{in} - V_{out}$

$V_{out} = g_{m1} V_{gs1} (r_{o1} \| r_{o2})$

$\Rightarrow V_{out} = (V_{in} - V_{out}) g_{m1} (r_{o1} \| r_{o2})$

$\Rightarrow V_{out} [1 + g_{m1} (r_{o1} \| r_{o2})] = V_{in} [g_{m1} (r_{o2} \| r_{o1})]$

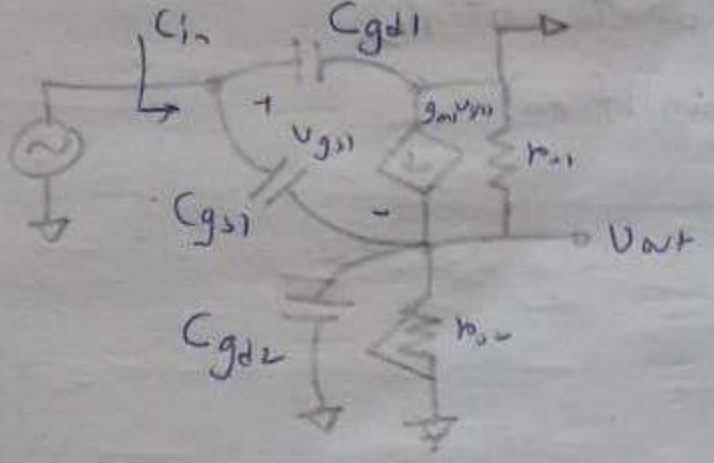
$\Rightarrow A_v = \frac{V_{out}}{V_{in}}$

$\Rightarrow$ $$A_v = \frac{g_{m1} (r_{o1} \| r_{o2})}{1 + g_{m1} (r_{o1} \| r_{o2})}$$

$g_{m1} (r_{o1} \| r_{o2}) \gg 1$

$\rightarrow \approx 1$ → Hence called source follower

Finding $C_{in}$: (Assuming $A_v \approx 1$)




$C_{gs1}$ → in and out connected

↓

Apply miller

$$C_{in} = C_{gs1}{}_{mill} + C_{gd1}$$

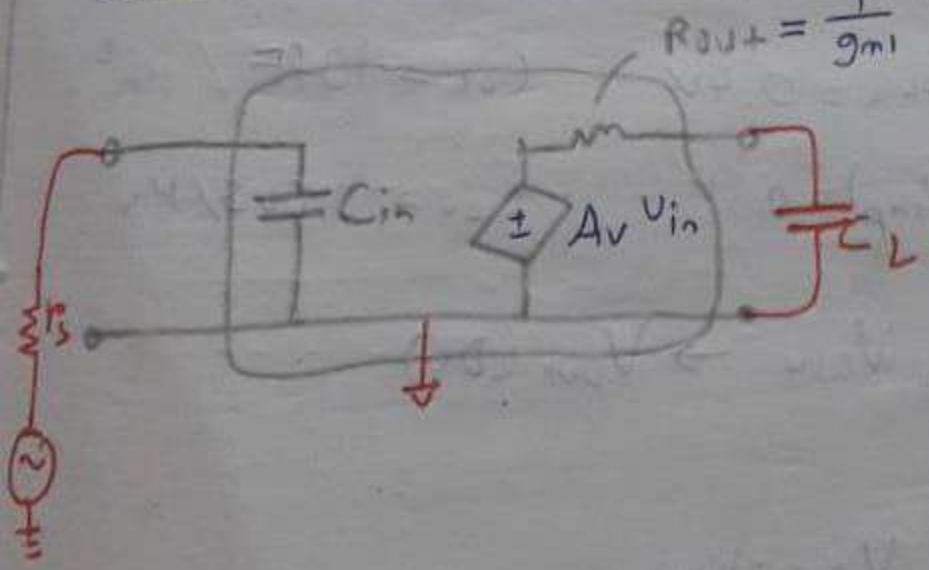
$= C_{gs1} (1 - A_v) + C_{gd1}$

$= C_{gs1} (1 - 1) + C_{gd1}$

$= C_{gd1}$ → Very small

$\therefore$ Small $C_{in}$, Small $R_{out}$

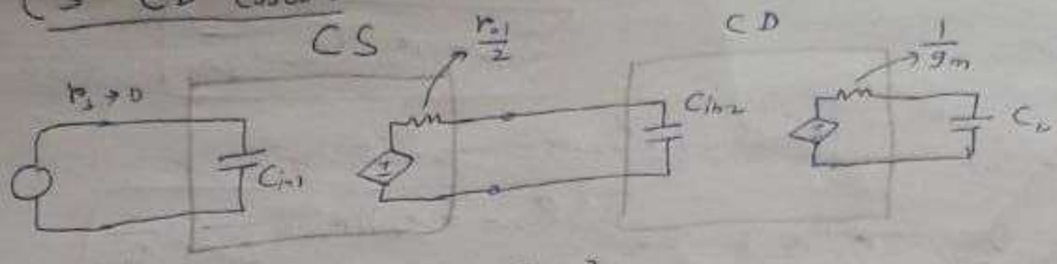
Bandwidth Calculation




$$B.W. = \min \left\{ \frac{1}{r_s C_{in}}, \frac{1}{R_{out} C_L} \right\}$$

$$= \left\{ \frac{1}{r_s C_{gd1}}, \frac{g_{m1}}{C_L} \right\}$$

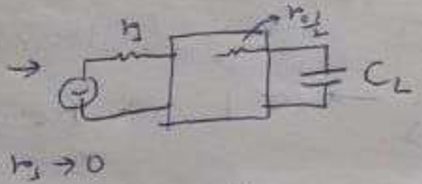
## CS-CD cascade




$$BW = \min\left\{\frac{2}{r_{o1} C_{in2}}, \frac{g_m}{C_L}\right\}$$

$$= \min\left\{\frac{2}{r_o C_{gd}}, \frac{g_m}{C_L}\right\}$$

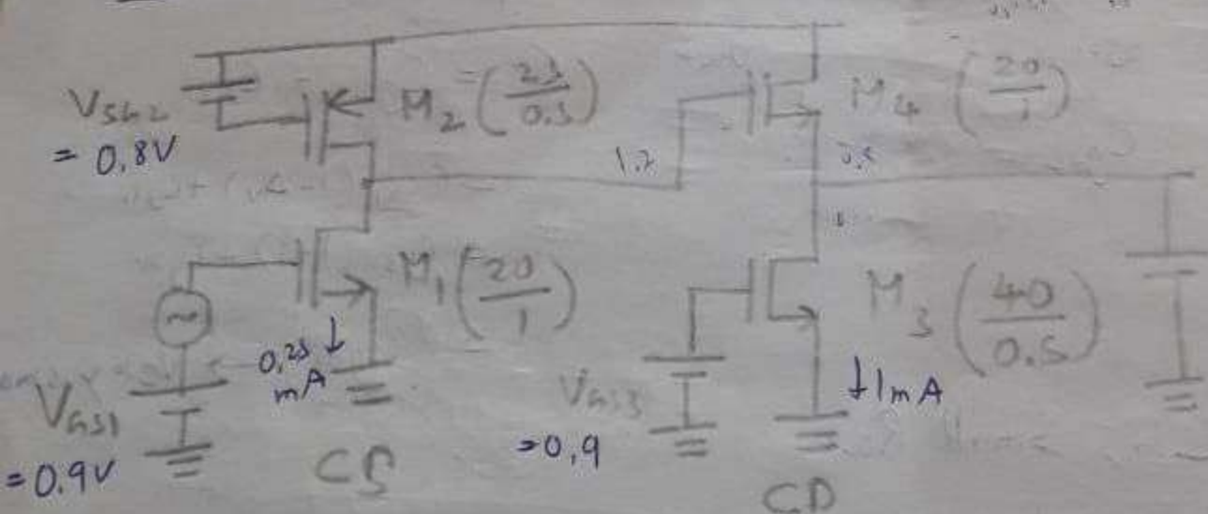
CD has helped to push the bandwidth further.

Only CS → 


$$BW = \frac{2}{r_{o1} C_L}$$ much higher than above 2 candidates

If needed, we can also use CD in 1st stage to reduce $r_s$ effect (if drastic at all).

## Numeric (CS-CD amplifier)




$\lambda = 0.01/L\,(\mu m)$

$K_n' = 0.1\,mA/V^2$ $\quad V_{thn} = 0.4V$ $\quad C_{ox} = 10fF/\mu m^2$

$K_p' = 40\mu A/V^2$ $\quad |V_{thp}| = 0.3V$ $\quad C_{ov} = 0.005/\mu m$

$I$ through $M_3$ determines $V_{GS4} \to V_{out}$ (DC)

in case $M_3$, $M_4$ in sat.

$$I_{D3} = 4 I_{D1} \quad \begin{cases} V_{GS1} = V_{GS3} \\ \left(\frac{W}{L}\right)_3 = 4\left(\frac{W}{L}\right)_1 \end{cases}$$

$I_{D3} = 1mA$

$(V_{GS4} - V_{th}) = 1V$

$\Rightarrow V_{GS4} = 1.5V$

$\downarrow$

$V_{out-cs} = 1.5V$

$\downarrow$

$V_{D3} = V_{S4} = 0.0V$

$M_3$ in triode

We need to change dimensions

Sol. → Increase $(\frac{W}{L})$ of $M_4$ to reduce $V_{GS4}$

$M_4: (\frac{40\,u}{0.5\,u}) \Rightarrow V_{GS4} = 1V$ → won't work (still $M_3$ triode)

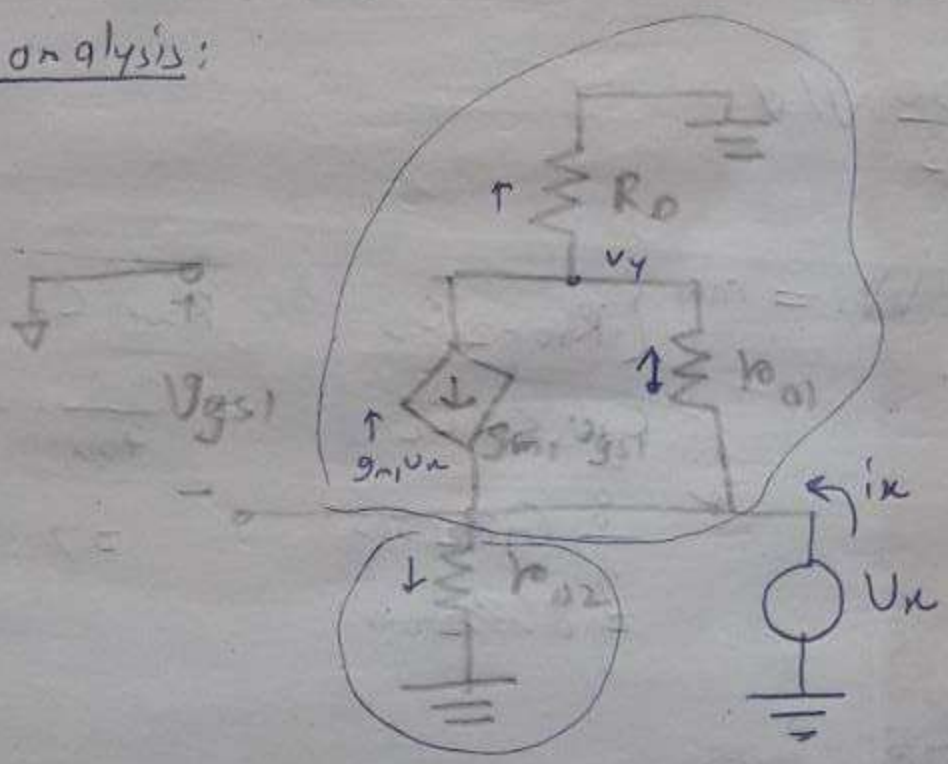
[Analyse yourself properly]

$M_4: (\frac{160\,u}{0.5\,u})$ → May ensure $M_3$ saturation.

Summary: Arbitrary selection of sizes may bring bias transistors into triode.

## Common Drain Amplifier with $R_D$:

### $R_{out}$ analysis:




$V_{gs1} = 0 - V_x$

$i_x = \frac{V_x}{r_{o2}} + \frac{V_x - V_y}{r_{o1}} + g_{m1} V_x$

$\frac{V_x}{r_{o2}} = \frac{V_y}{R_D}$ · $V_y = \frac{R_D}{r_{o2}} V_x$

$g_m V_x + \frac{V_x - V_y}{r_{o1}} = \frac{V_y}{R_D}$

$(g_m + \frac{1}{r_{o1}}) V_x = \frac{V_y}{r_{o1} \| R_D}$

$i_x = V_x \left( \frac{1}{r_{o2}} + \frac{1}{r_{o1}} + \cancel{\quad} - \frac{(g_m + \frac{1}{r_{o1}})}{r_{o1} \| R_D} + g_{m1} \right)$

$\sim \left(\frac{2}{g_{m1}}\right)$ ..

↑

$$R_{OUT} = \left( \frac{R_D + r_{o1}}{1 + g_{m1} r_{o1}} \right) \| r_{o2}$$

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Previous day numeric

↳ $M_4 = \frac{160n}{0.5n}$ → $V_{GS4} = 0.65V$, $V_{out} = 0.55V$

Repeat same example But $W_4 = 160\mu m$, $L_4 = 0.5\mu m$

$I_{DS1} = 0.25mA$ $I_{DS3} = 1mA$ $V_{DS1} = 1.2V$ ↴

$\lambda_1 V_{DS1} = \lambda_2 V_{SD2}$ $(V_{DS1} + V_{SD2} = V_{DD})$

$V_{GS4} = 0.65V \Rightarrow V_{OUT} = V_{DS1} - V_{GS4}$

$= 1.2 - 0.65 = 0.55V$

$g_{m1} = 1mA/V$

$R_{out1} = \frac{400}{3}\Omega$ $R_{out2} = \frac{1}{g_{m4}} = \frac{1}{8}k\Omega$

$A_V = -\frac{400}{3} V/V$

$B.W. = \min\left\{\frac{1}{R_{out2} C_L}, \frac{1}{R_{out1} C_{total2}}\right\}$ ..

$C_{gd3} << C_L$

$C_{in2} = C_{gd4}$

$= 0.005 \times 160$

$= 0.8fF$

$= \frac{3}{400} \times 10^{-3} \times (1.025 \times 10^{-15})^{-1}$

$= \frac{8}{1} G$ rads$^{-1}$

$= 8$ G rads$^{-1}$

$= 7.31$ G rads$^{-1}$

$C_{total2} = C_{in2} + C_{gd2} + C_{gd1}$

$= 0.005(160 + 25 + 20)$

$= 1.025fF$

$V_{out}$ of Last stage

(Limited swing)

Supply voltage is restricted

$(V_{GS4\,min})$

0.65V ------

0.55V ——— ↑ 1V

0.5V ------ ↓ 0.05V

$(V_{DS3\,min})$

# Common Gate Amplifier

- It gives $A_i = 1$ current gain
- Voltage amplifier
- Input = Current
- Output = Voltage

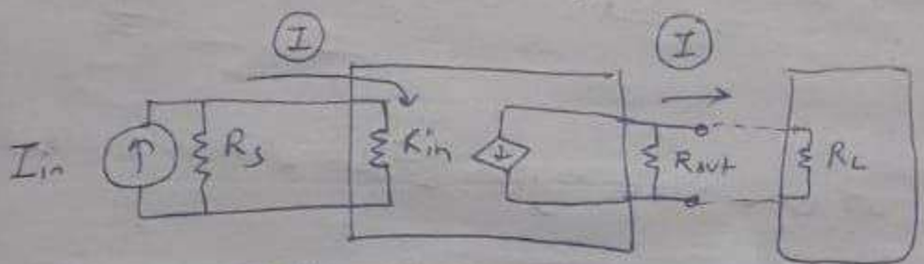
Transimpedance amplifier

CS :- Av

CD :- $R_{out}\downarrow$, $C_{in}\downarrow$ (Buffer for Voltage Mode)

CG :- $R_{out}\uparrow$, $R_{in}\downarrow$ (Buffer for Current Mode)

Purpose: Small $R_{in}$, Large $R_{out}$




$R_{in}\downarrow$ => Entire current goes into it.

($R_{in} \ll R_s$)

Current

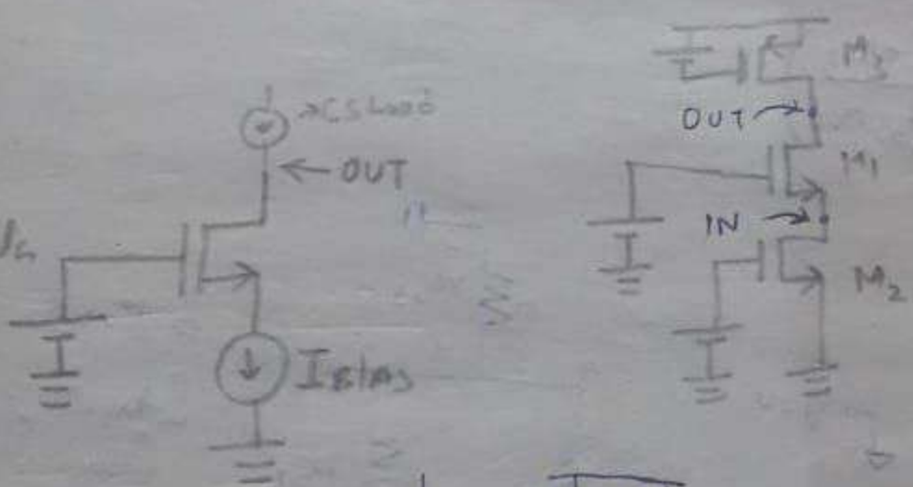
No current into Rout ↓

Fully feeds 2nd stage

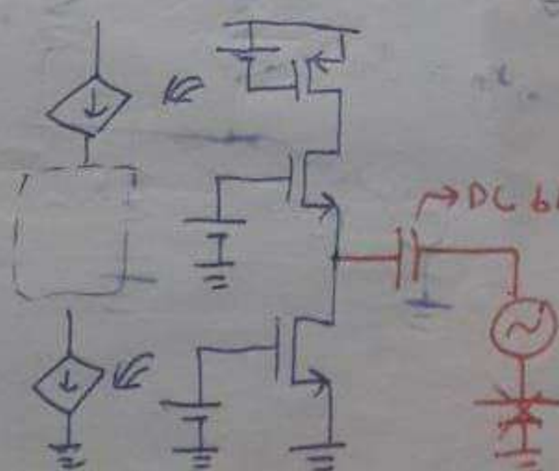
($R_L \ll R_{out}$)

$R_L\uparrow$

## Basic configuration, Biasing and Operation




O/p can also be taken as Voltage but Rout is large so B.W.↓



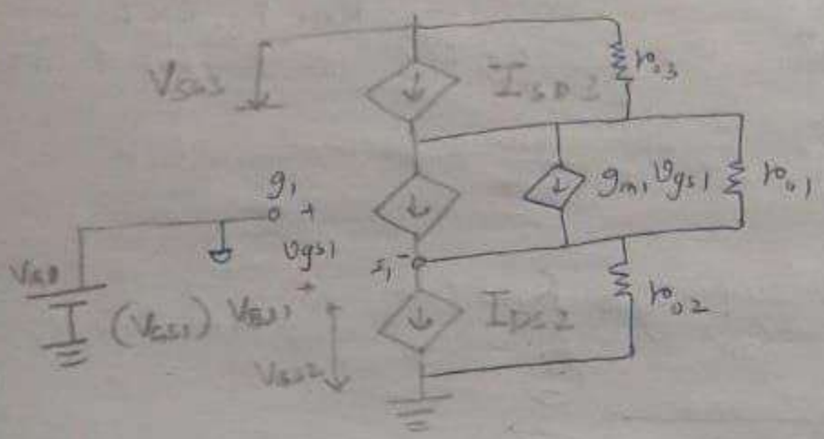

Both currents must be agreeing

DC blocking cap. (B.W.↓)

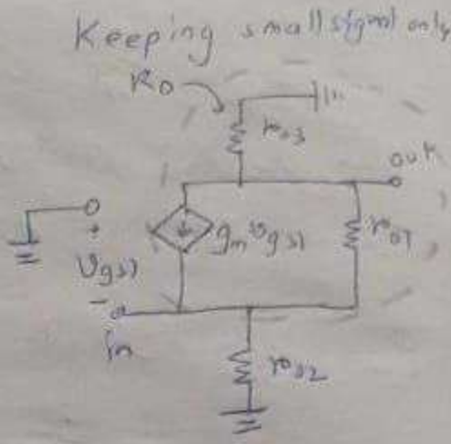
→ meaningful DC voltage (no needed if DC block cap is used

## Small Signal Equivalent

For simplicity, we replace PMOS by ideal current source with a resistance




Keeping small signal only:

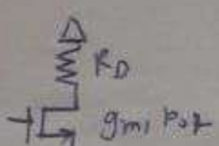



**$R_{in}$:**

Impedance of encircled region [From previous class]

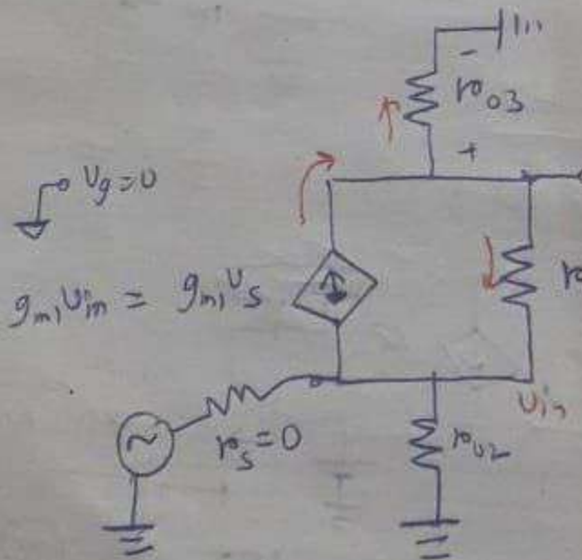
$$\left(\frac{R_D + r_{o1}}{1 + g_m r_{o1}}\right) \rightarrow \left(\frac{R_{o3} + r_{o1}}{1 + g_{m1} r_{o1}}\right)$$

$$\therefore \quad R_{in} = r_{o2} \parallel \frac{(r_{o3} + r_{o1})}{1 + g_{m1} r_{o1}} \sim \frac{2}{g_{m1}} \rightarrow R_{in} \text{ is small}$$




$$\equiv \left(\frac{R_D + r_{o1}}{1 + g_{m1} r_{o1}}\right)$$

**$A_V$:**




$V_{out} \approx r_{o3} g_{m1} V_{in}$

[Assuming most of it flows through $r_{o3}$]

$V_{out} \gg V_{in}$

$\therefore$ $r_{o1}$ ~~current~~ $\rightarrow$ $V_{out} \rightarrow 0$

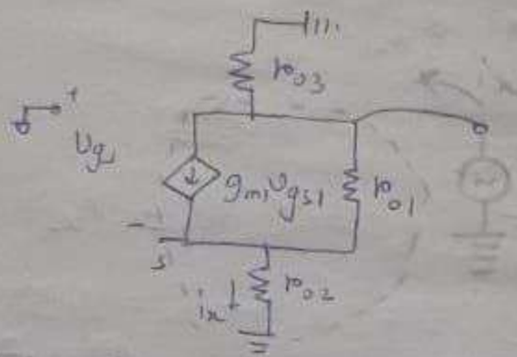
$$V_{out} = (g_m r_{o3} V_{in}) * \frac{r_{o1}}{r_{o1} + r_{o3}}$$

Current division

$V_{out} = (r_{o3} g_{m1}) V_{in} \times \frac{r_{o1}}{r_{o1} + r_{o3}}$

$A_V = \frac{V_{out}}{V_{in}} = g_{m1} (r_{o3} \| r_{o1})$ → I/p, o/p in phase

**Rout:**




(As a current input at source) [Current mode op]

First find impedance of encircled part and then $\| r_{o3}$

$V_S = i_x r_{o2}$

$V_{gs1} = 0 - V_S$
$= - i_x r_{o2}$

$i_x = g_{m1} V_{gs1} + \frac{V_x - i_x r_{o2}}{r_{o1}}$

$\Rightarrow i_x = g_{m1} (-i_x r_{o2}) + \frac{V_x}{r_{o1}} - \frac{i_x r_{o2}}{r_{o1}}$

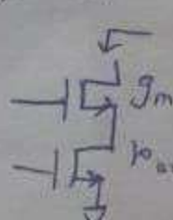
$\Rightarrow i_x \left(1 + g_m r_{o2} + \frac{r_{o2}}{r_{o1}}\right) = \frac{V_x}{r_{o1}}$

$\Rightarrow \frac{V_x}{i_x} = \frac{r_{o1}}{\left(1 + g_m r_{o2} + \frac{r_{o2}}{r_{o1}}\right)^{-1}} = r_{o1} \left(1 + g_m r_{o2} + \frac{r_{o2}}{r_{o1}}\right)$

$= r_{o1} + r_{o2} + g_m r_{o1} r_{o2}$

$R_{out} = (r_{o1} + r_{o2} + g_{m1} r_{o1} r_{o2}) \| r_{o3} \sim (g_{m1} r_{o1} r_{o2}) \| r_{o3}$

Considering lower circuit below $V_{out}$, $R_{out}$ is very large → $g_{m1} r_{o1} r_{o2}$
(Intrinsic gain) × $r_{o2}$



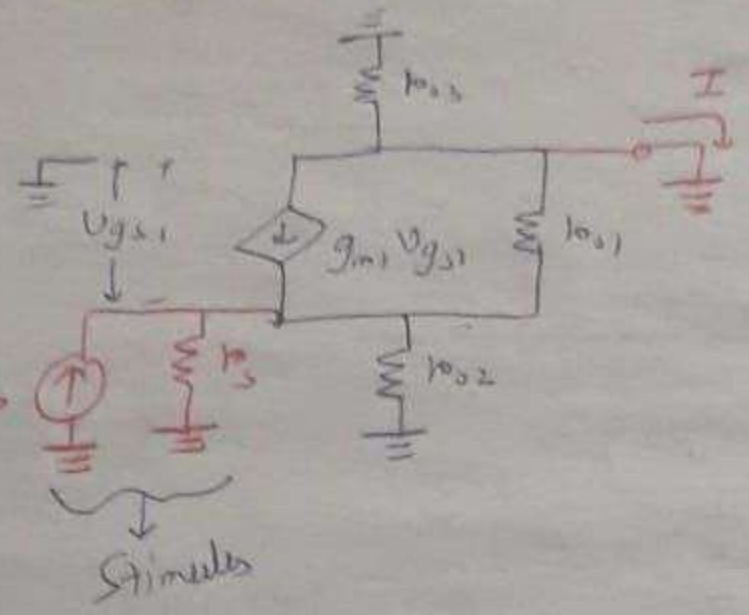

$(g_{m1} r_{o1} r_{o2}) + r_{o1} + r_{o2}$

** In reality $V_{in}$ is shorted [Voltage mode operation] → so $r_{o2}$ goes out

$r_s = 0$ → $R_{out} = r_{o3} \| r_{o1}$

$R_{out}$ — V mode → $r_{o3} \| r_{o1}$
— Current mode → $(r_{o1} + (r_{o2} \| r_{o3})(1 + g_m r_{o1})) \| r_{o3}$

# CG Amplifier as a Current Amplifier




o/p port unloaded (short to ground)

**$R_{in}$:**

$$R_{in} = r_{o2} \,||\, \frac{r_{o3} + r_{o1}}{1 + g_{m1} r_{o1}}$$

or

$$\frac{r_{o1}}{} \,||\, \frac{r_{o2}}{} \,||\, \frac{1}{g_{m1}}$$

**$A_i$:** $r_s \to \infty$

$$A_i = \frac{r_{o2}}{r_{o2} + r_{o1} \,||\, \frac{1}{g_m}} \approx 1$$

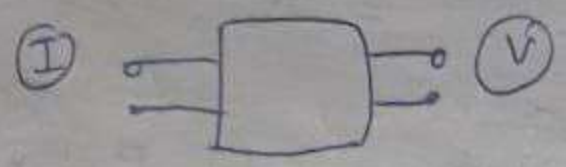
$r_s \not\to \infty$ $\quad A_i = (?) \longrightarrow$

$$\frac{r_{o2} \,||\, r_s}{r_{o2} \,||\, r_s + \frac{1}{g_m} \,||\, r_{o1}}$$

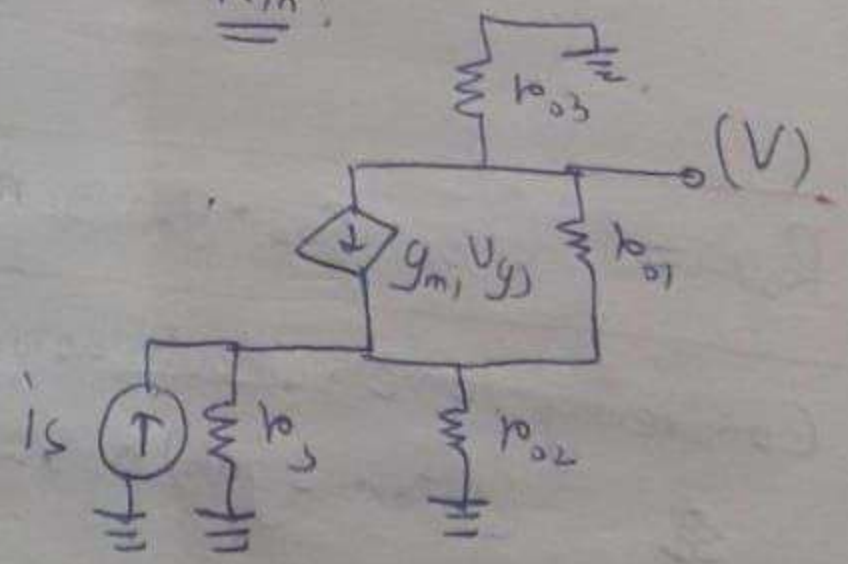
**$R_{out}$:**

$$R_{out} = \left( r_{o1} + r_{o2} \,||\, r_s \right) \,||\, r_{o3} \left( + g_{m1} r_{o1} (r_s \,||\, r_{o2}) \right)$$

## CG Amp. as Trans-Impedance Amplifier




**$R_{in}$:**




$$R_{in} = r_{o2} \,||\, \frac{r_{o3} + r_{o1}}{(1 + g_{m1} r_{o1})}$$

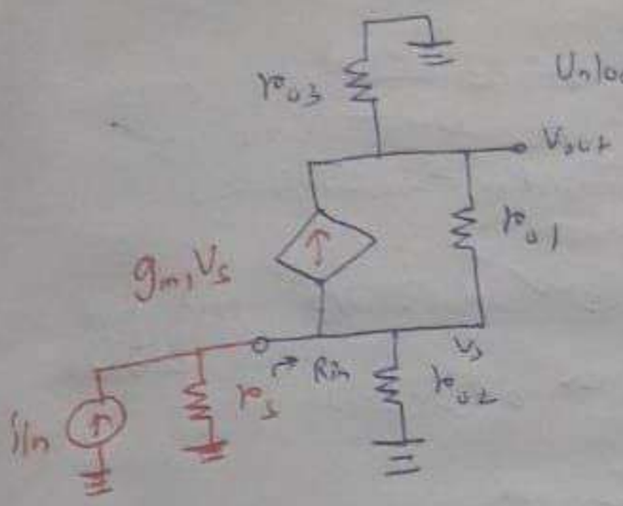
**$Z_m$:**

$$\left. \frac{v_o}{i_s} \right|_{R_s \to \infty} =$$

**$R_{out}$:**

Week-4 (21/9/20)

## Trans-impedance amplifier (CG stage)




Unloaded o/p port

Analysis 1. $R_{in}$ =

$$R_{in} = r_{o2} \,||\, \left(\frac{r_{o1} + r_{o3}}{1 + g_{m1} r_{o1}}\right) \approx \frac{2}{g_{m1}}$$

↳ $r_{o3}$, $r_{o1}$ comparable

Analysis for $Z_m$ =

$r_s >> R_{in}$: Current division

$$V_{out} = r_{o3} \times i_{in} \times \frac{r_{o2}}{r_{o2} + \left(\frac{r_{o3} + r_{o1}}{1 + g_{m1} r_{o1}}\right)}$$

$$Z_m = \frac{V_{out}}{i_{in}} = r_{o3}\left[\frac{r_{o2}}{r_{o2} + \left(\frac{r_{o3} + r_{o1}}{1 + g_{m1} r_{o1}}\right)}\right] \approx r_{o3}$$

If we short $V_{out}$ and check for $I_{out}$:

$$A_i = \frac{r_{o2}}{r_{o2} + \left(\frac{r_{o3} + r_{o1}}{1 + g_{m1} r_{o1}}\right)} \approx 1$$

→ $r_{o3}$, $r_{o1}$ comparable.

If $r_{o3} >> r_{o1}$ ⇒ Our approx. are wrong

**

For $r_{o3} \to \infty$, $R_{in} = r_{o2} \,||\, \infty$

[Very high imp. n/w] ↳ No path for current

Practically if $r_{o3} \sim g_m r_o^2$ ⇒ $R_{in} = r_{o2} \,||\, r_o$

Analysis for $R_{out}$ =

$r_s \to \infty$ :

$$R_{out} = r_{o3} \,||\, \{r_{o2} + r_{o1} + g_{m1} r_{o1} r_{o2}\} \approx r_{o3}$$

$$Z_m = A_I\Big|_{\substack{\text{unloaded}\\(V_{out}=\downarrow)}} \times \overset{(R_{out})}{r_{o3}} \rightarrow r_3$$

CS, CD → High $R_{in}$ (Input as voltage)

∴ Input cannot be current source

[∵ No current amplifier, trans-impedance]

But CS → Transconductance ✓ (o/p impedance high ↓ current)

[$G_m = g_{m1} \rightarrow i_o = g_m v_{gs1}$]

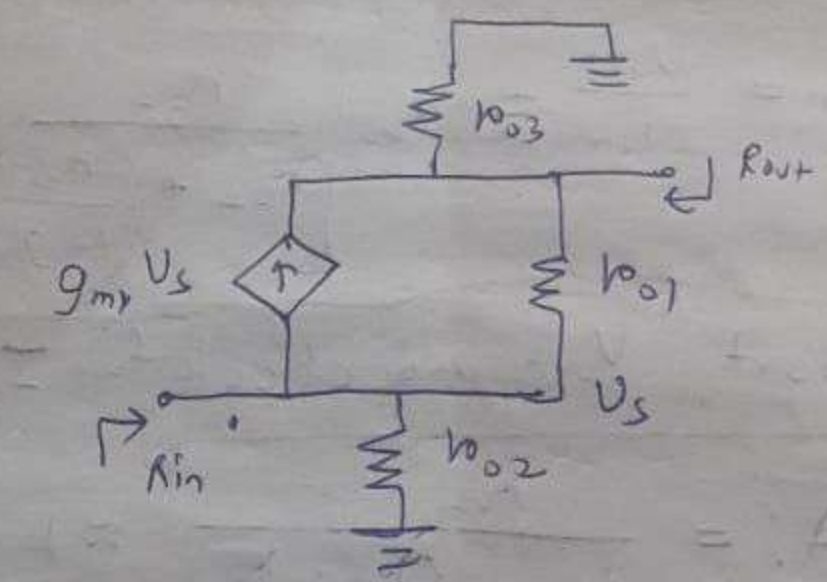
CD → $R_{in}$ high, $R_{out}$ low

↳ Cannot use current o/p

[∵ No o/p i possible]

## Summary

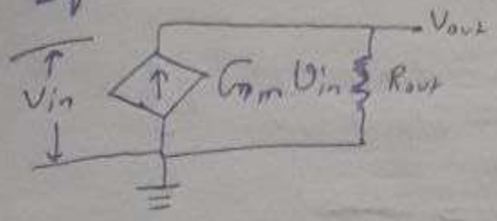
Small signal equivalent →




1. Voltage Amp. (Small $R_s$)

- $R_{in} = r_{o2} \| \left( \dfrac{r_{o1} + r_{o3}}{1 + g_{m1} r_{o1}} \right) \approx \dfrac{2}{g_{m1}}$
- $R_{out} = r_{o1} \| r_{o3}$ [$R_s \rightarrow 0$; Voltage in – short]
- $A_v = g_{m1} (r_{o1} \| r_{o3})$ [$G_m R_{out}$]

Equivalent model 2




$V_{out} = G_m R_{out} V_{in}$

2. Current Amp. (Large $R_s$)

- $R_{in} = r_{o2} \| r_{o1} \| \frac{1}{g_m}$

[o/p → short]

- $R_{out} = r_{o3} \| \{r_{o1} + r_{o2} + g_{m1} r_{o1} r_{o2}\} \approx r_{o3}$
- $A_I \approx \frac{r_{o2}}{r_{o2} + \left(\frac{r_{o1} + r_{o3}}{1 + g_{m1} r_{o1}}\right)} \approx 1$

3. Trans-Imp. Amp (Large $R_s$)

- $R_{in} = r_{o2} \| r_{o1} \| \frac{1}{g_m}$
- $R_{out} = r_{o3} \| \{r_{o1} + r_{o2} + g_{m1} r_{o2} r_{o1}\} \approx r_{o3}$
- $Z_m = r_{o3} \left\{ \frac{r_{o2}}{r_{o2} + \left(\frac{r_{o1} + r_{o3}}{1 + g_{m1} r_{o1}}\right)} \right\} = [R_{out}][A_I]$

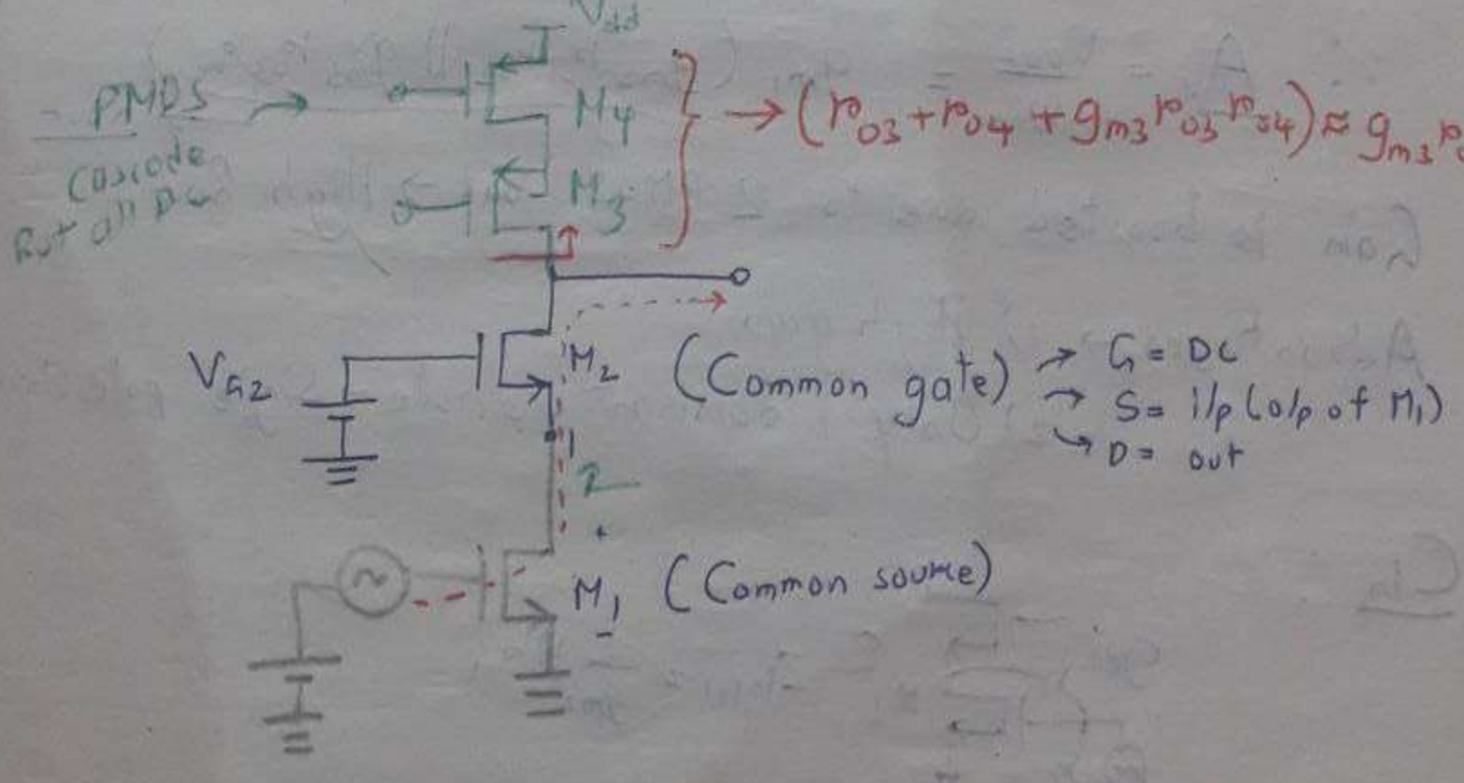
This ckt is flexible in terms of the kind of signal used at i/p or o/p.

## CS-CG or Cascode Amplifier

### Basic Configuration

(PMOS) (NMOS)

Both load and amp. site are cascode


$V_{dd}$
PMOS → Cascode Rout all DC
$M_4$
$M_3$
$\rightarrow (r_{o3} + r_{o4} + g_{m3} r_{o3} r_{o4}) \approx g_{m3} r_{o3} r_{o4}$
$V_{G2}$
$M_2$ (Common gate) → G = DC, S = i/p (o/p of $M_1$), D = out
$M_1$ (Common source)

How is signal coupled from CS to CG?

Ans: Current coupling [∵ CS o/p → high imp. ; CG i/p → low]

$R_{out}(CS) = r_{o1}$ ; $R_{in}(CG) \approx \frac{1}{g_{m2}}$

Efficient current coupling

If I want to find o/p current $i_o$ :- (short $V_{out}$)

$i_o = (g_{m1} V_{in}) \times 1$

↓ CS stage current ; ↓ CG stage current gain

∴ Transconductance of cascode $= G_m = \frac{i_o}{V_{in}} = g_{m1}$

Now we remove short and we find $V_{out}$ =

$V_{out} = i_o \times R_{out}$(cascode load - CS-CG)

$= i_o \times \{ r_{o1} + r_{o2} + g_{m2} r_{o2} r_{o1} \} \| \{ r_{o3} + r_{o4} + g_{m3} r_{o3} r_{o4} \}$

$\approx i_o \times (g_{m2} r_{o1} r_{o2}) \| (g_{m3} r_{o3} r_{o4})$

$\approx g_{m1} [(g_{m2} r_{o1} r_{o2}) \| (g_{m3} r_{o3} r_{o4})] V_{in}$

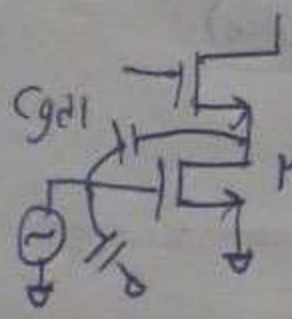
∴ $\underline{A_V} = \frac{V_{out}}{V_{in}} = g_{m1} \underbrace{(g_{m2} r_{o1} r_{o2} \| g_{m3} r_{o3} r_{o4})}_{\rightarrow \underline{R_{out}}}$

Gain is boosted due to 2 PMOS Load → High $R_{out}$

Advantages → 1) High gain

2) Only 1 dominant o/p node → Single pole chara.

<u>Cin</u>




$Z_{in(1)} = \frac{1}{g_{m2}} \| r_{o1}$

$V_{d1} = V_{in}\, g_{m1}\, R_{out-1}$

Drain node of $M_1$ $= V_{in}\, g_{m1} \left(\frac{1}{g_{m2}}\right)$ → Applicable when $C_L$ shunts the o/p at mid and high freq.

→ Not exact [We have PMOS load above]

$\therefore \frac{V_{d1}}{V_{in}} = \frac{g_{m1}}{g_{m2}} \simeq 1$

→ $C_{gd1}$ experiences negligible miller multiplication

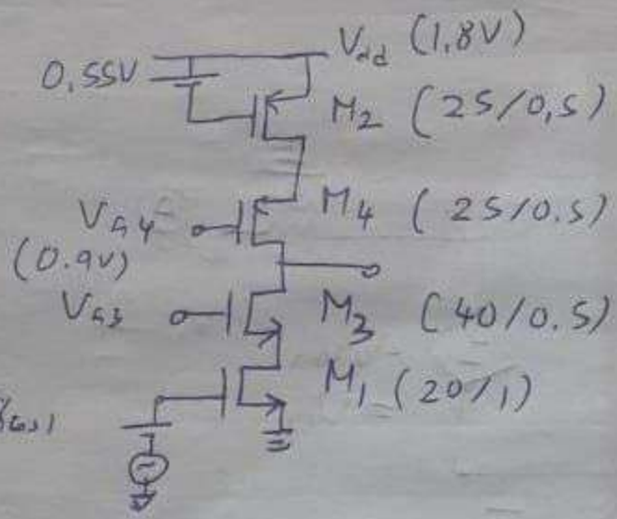
$\therefore C_{in} = C_{gs1} + C_{gd1}\left(1 + \frac{V_{d1}}{V_{in}}\right)$

$= C_{gs1} + 2C_{gd1}$

cap

Another advantage: Input to cascode is very low.

Numeric (Assignment-3)




$\lambda = \frac{0.01}{L(\mu m)}$

$C_{ox} = 10fF/(\mu m \times \mu m)$

$C_{ov} = 0.005\ /\mu m$

$C_L = 1pF$

Find:-
1) Av
2) $C_{in}$
3) $R_{out}$

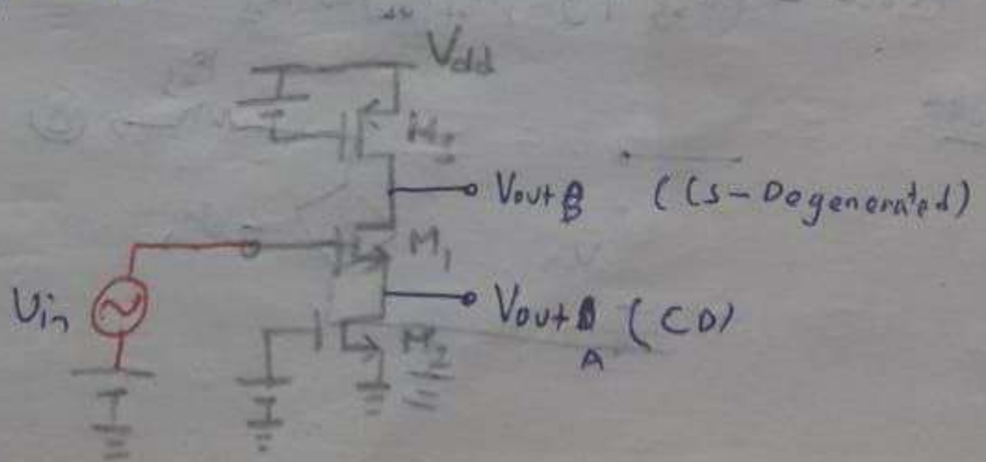
Compare with CS amp. (w/o $M_3, M_4$)

22/9/20

## Differential Amplifier

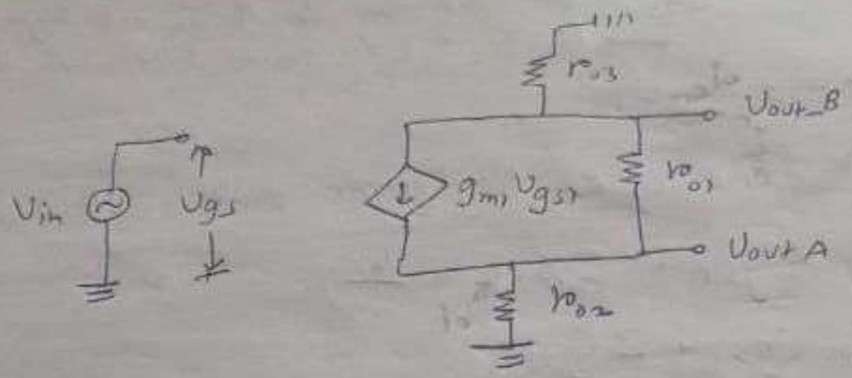
### Construction of Differential amplifier

CD/CS amplifier:



Ⓐ

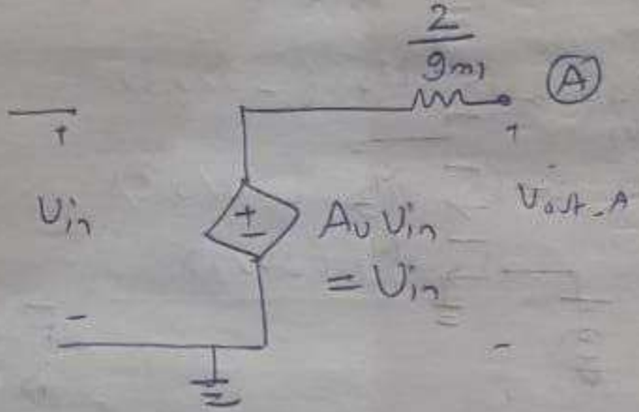
Small signal




Ⓐ : $A_V \approx 1$

$$R_{out} = r_{o2} \| \left( \frac{r_{o3} + r_{o1}}{1 + g_{m1} r_{o1}} \right) \approx r_{o2} \| \frac{2}{g_{m1}} \approx \frac{2}{g_{m1}}$$

Eq. ckt



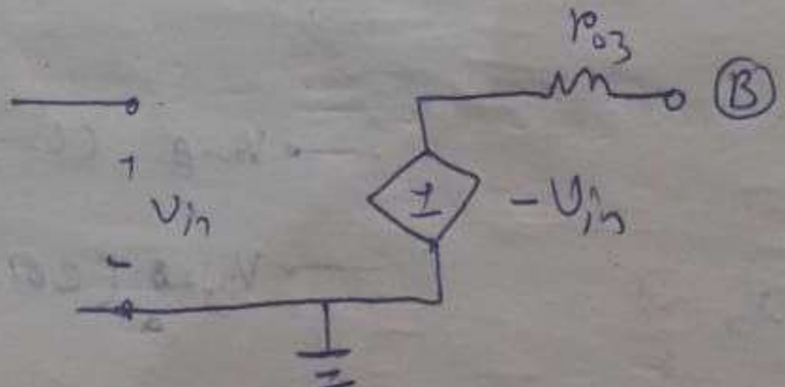

Ⓑ : $A_V \approx -G_m R_{outB} \approx -\left( \frac{g_{m1}}{1 + g_{m1} r_{o2}} \right) (r_{o3} \| g_{m1} r_{o1} r_{o2})$

$G_m \triangleq \frac{i_{sc}}{V_{in}}$

$$\approx -\frac{g_{m1} r_{o3}}{g_m r_{o2}} = -\frac{r_{o3}}{r_{o2}} \approx -1$$

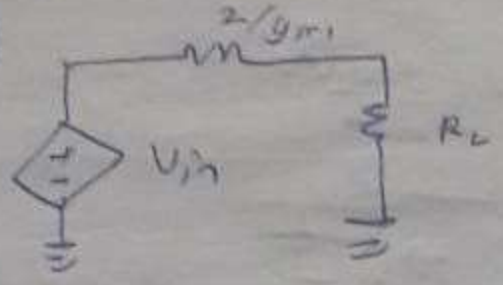
$$R_{out} \simeq (r_{o3} \| g_{m1} r_{o1} r_{o2}) \approx r_{o3}$$

Eq. ckt



If $V_{out\_A}$ is loaded by $R_L$ →

(A)




Voltage division
↳ Attenuation of $V_{out\_A}$

(B) → $A_V = \dfrac{-g_{m1}}{(1+g_{m1}(r_{o2}\|r_L))} (r_{o3}\| g_m r_{o1} r_{o1}\|r_L)$

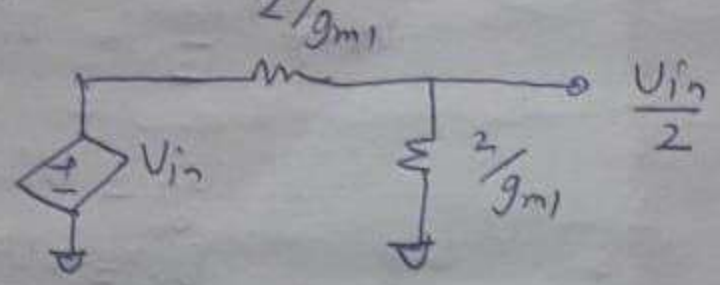
Extreme: $r_L \to 0$ $\quad A_V = -g_{m1}(r_{o1}\|r_{o3})$

$R_{out} \to r_{o3}\|r_{o1}$

Transconductance increases from $\frac{1}{r_{o2}}$ to $\frac{g_{m1}}{1+g_m r_{o2}}$

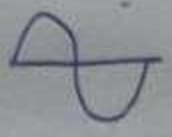
If $R_L \to \frac{2}{g_m}$

(A)

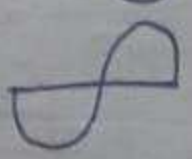



(B) $A_V = -\dfrac{g_{m1}}{2}(r_{o3}\|r_{o1})$

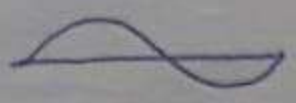
Initially b4 $R_L$ is applied.

signal at $V_{in}$ 

signal at $V_{out\,A}$

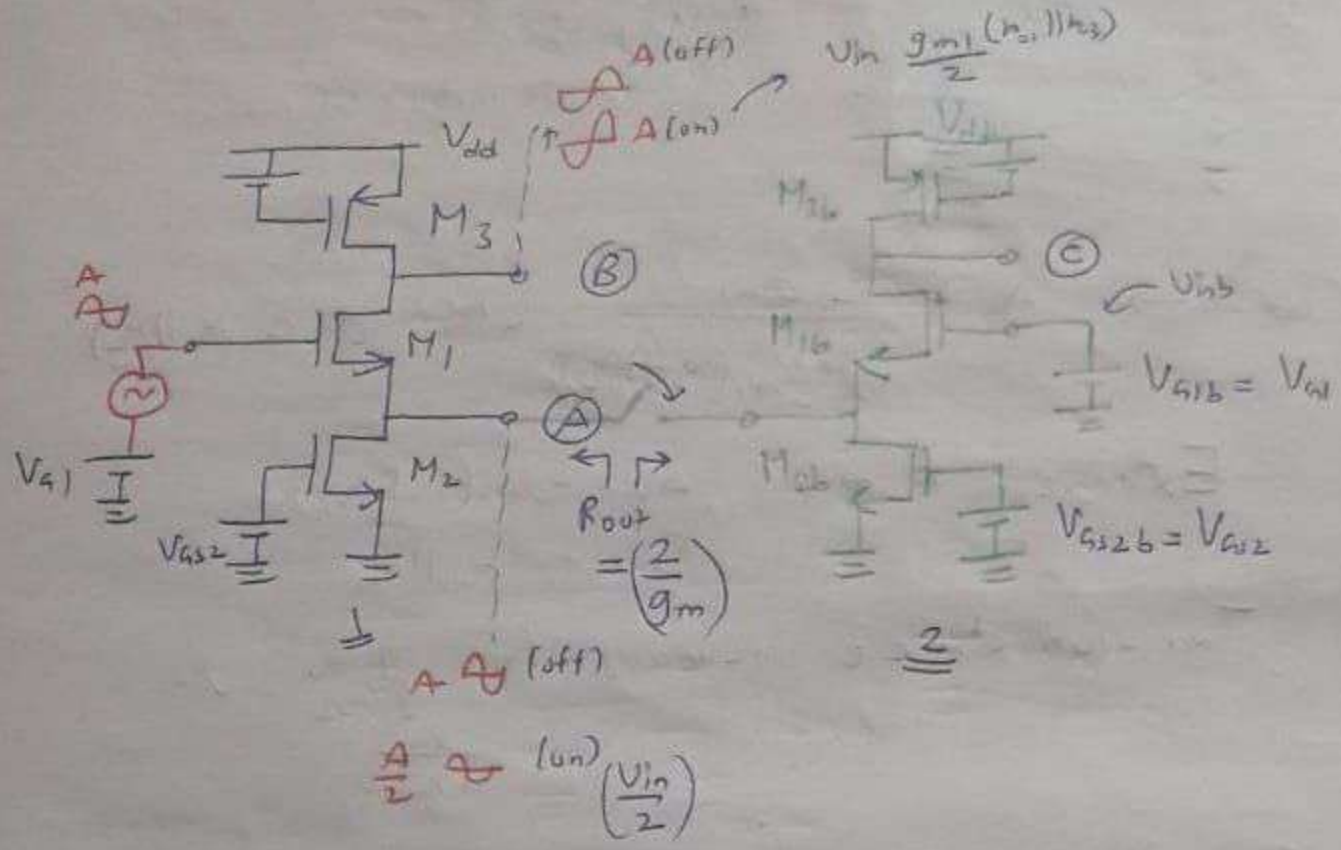
signal at $V_{out\,B}$ 

Now $R_L = \frac{2}{g_m}$

$V_{out\_A}$  ↓ 1/2

$V_{out\_B}$ ↑ 2

# (CD/CS) - CG amplifier




switch off → on

$V_{out\,B} \rightarrow \left(\frac{1}{2}\right)\downarrow$

$V_{out\,A} \rightarrow$ (Big) ↑

Why $\frac{1}{2}$ in $V_{in}\frac{g_{m1}}{2}(r_{o1}\|r_{o3})$ !

$\because$ $V_g = V_{in}$, $V_S = -\frac{V_{in}}{2}$ $\rightarrow V_{gs} = \frac{V_{in}}{2}$

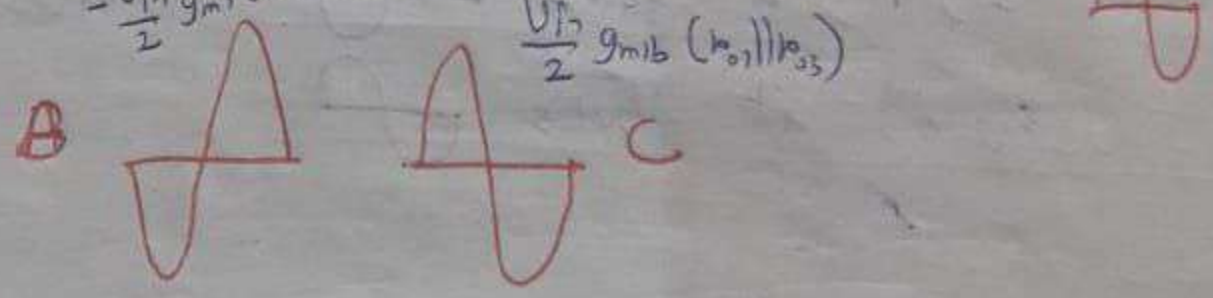
For 2 → CG amp.

(A) → i/p

(C) → o/p

$$A_V = \frac{V_{out\,c}}{V_A} = g_{m1b}(r_{o3}\|r_{o1})$$

$$V_{out\,c} = \frac{V_{in}}{2} g_{m1b}(\ldots)$$




$$V_{out\_c} = -V_{out\_B} = \frac{V_{in}}{2} g_{m1}(r_{o3}\|r_{o1})$$

$$A_V = \frac{g_{m1}}{2}(r_{o3}\|r_{o1})$$

From 1 signal we generate 2 signals of opposite phase and amplified.

Now $V_{in\_b}$ is applied, we do superposition →

$$V_{out\_b} = -(V_{in\_a} - V_{in\_b}) \frac{g_{m1}}{2} (r_{o1} \| r_{o3})$$

$$V_{out\_c} = (V_{in\_a} - V_{in\_b}) \frac{g_{m1}}{2} (r_{o1} \| r_{o3})$$

} → 180° apart

$$\therefore V_{out\_c} - V_{out\_b} = (V_{in\_a} - V_{in\_b}) \cdot g_{m1}(r_{o1} \| r_{o3}) = \Delta V_{out}$$

sole o/p

$$\Delta V_{out} = 2 A_v (V_{ina} - V_{inb})$$

↓ solve

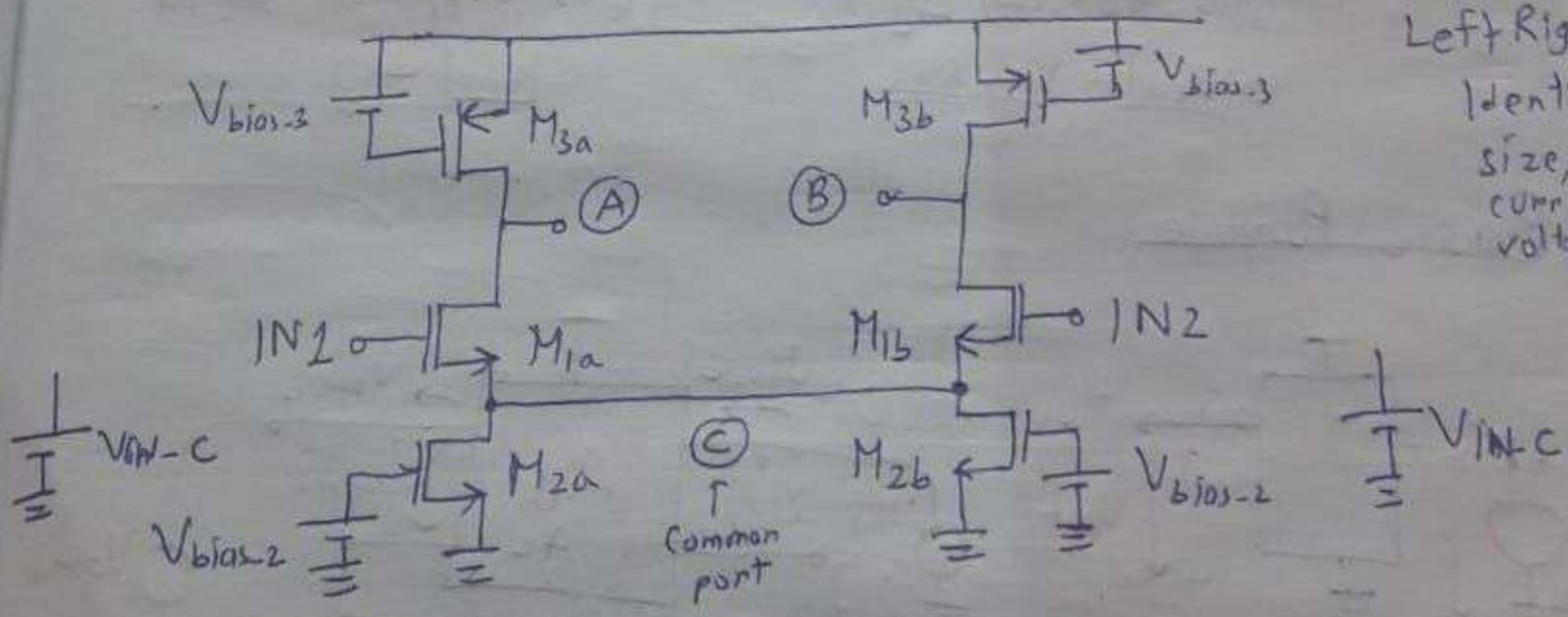
$$\Delta V_{out} = 2 A_v \Delta V_{in}$$

$$\boxed{A_{diff} = \frac{\Delta V_{out}}{\Delta V_{in}} = 2 A_v}$$

$$A_v = -\frac{g_m (r_{o1} \| r_{o3})}{2}$$

CD/CS cascaded with CG ≡ Differential Amplifier

## Biasing Constraints:



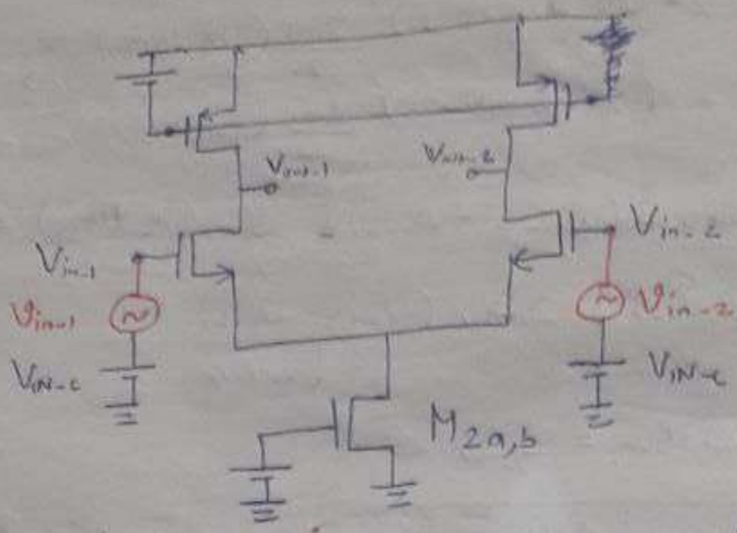

Left Right ↴ Identical size, current, voltages

$$\boxed{I_{DS1} = I_{SD3} = I_{DS2}}$$

↳ Constraint to satisfy

$V_{GS-1}$ gets self adjusted based on $I_D$, sizes ↴ Should not put $M_2$ into triode.

$V_{IN-C}$ has a range within which $M_2$, $M_3$ are in saturation → It has to be kept in mind.
This range is called Input Common Mode Range (ICMR)




$V_{out_d} = V_{out-1} - V_{out-2}$

$V_{in_d} = V_{in-1} - V_{in-2}$

$V_{out_d} = A_d \cdot V_{in_d}$

↓

Differential mode

(To improve) $A_d$ ↑↑

Ideal – Very high

$V_{in-C} = \frac{V_{in1} + V_{in2}}{2}$

$V_{out-C} = \frac{V_{out1} + V_{out2}}{2}$

$V_{out-C} = A_C \cdot V_{in-C}$

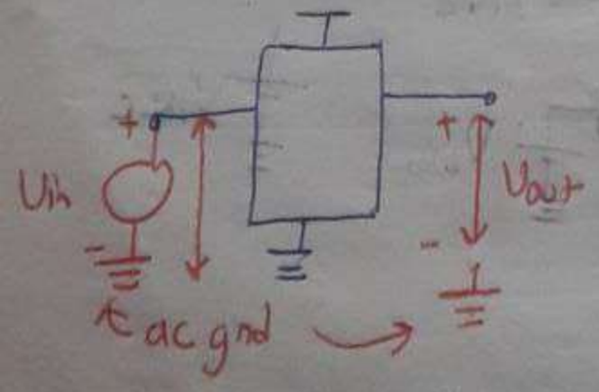
↓

Common mode

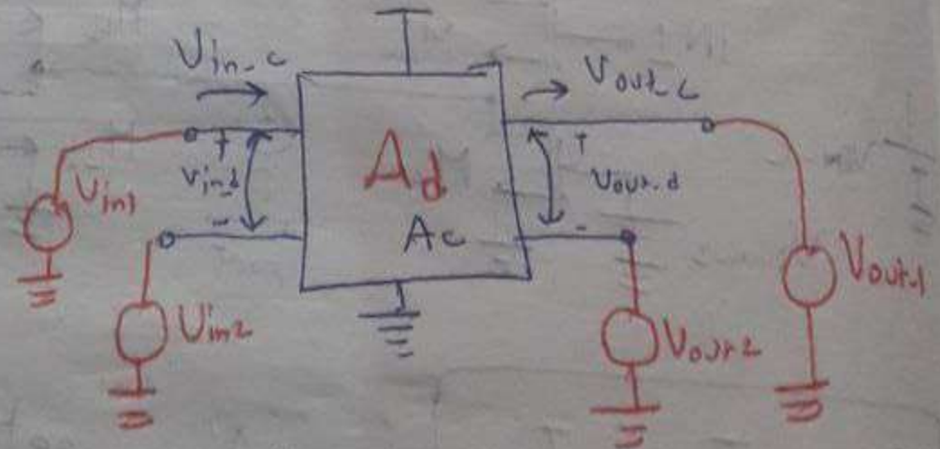
(To suppress) $A_C$ ↓↓

Ideal – 0

## Basic Purpose




Single-ended




Differential

$V_{out-d} = A_d V_{in-d}$

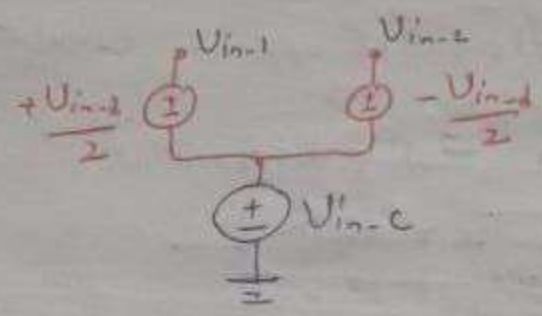
$V_{out-C} = A_C V_{in-C}$

Range (ICMR)

## Signal Pair – Differential and Common mode Components

$$V_{in-d} = V_{in-1} - V_{in-2}$$
$$V_{in-c} = \frac{V_{in-1} + V_{in-2}}{2}$$

$$\rightarrow \quad V_{in-1} = V_{in-c} + \frac{V_{in-d}}{2}$$
$$V_{in-2} = V_{in-c} - \frac{V_{in-d}}{2}$$




### Non-ideal parameters:–

Not the complete ← point

$$V_{out-d} = A_{cd}\, V_{in-c}$$
$$V_{out-c} = A_{dc}\, V_{in-d}$$

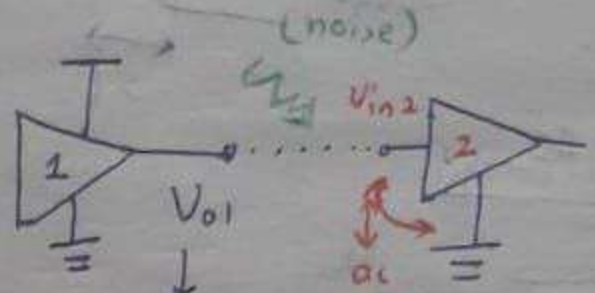
We have to take $A_d$, $A_c$, $A_{dc}$, $A_{cd}$ → combined effect

$$V_{out-c} = A_{dc}\, V_{in-d} + A_c\, V_{in-c}$$
$$V_{out-d} = A_{cd}\, V_{in-c} + A_d\, V_{in-d}$$

our aim ⇒ $\underbrace{A_{cd}, A_{dc}, A_c}$ assume 0

How do we ensure? [Identical left, right half] ← Unless stated

## Need of Differential signalling (system perspective):



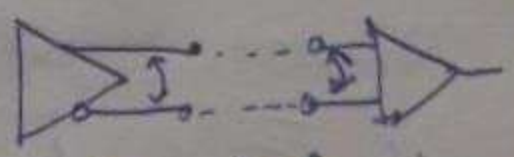

wrt ac gnd ↔ If not equal, ~200mV we have an equivalent noise [Wrong perception of signal generated & produced]

rcvd. signal = Vout + noise

↓

2 accepts it as a signal

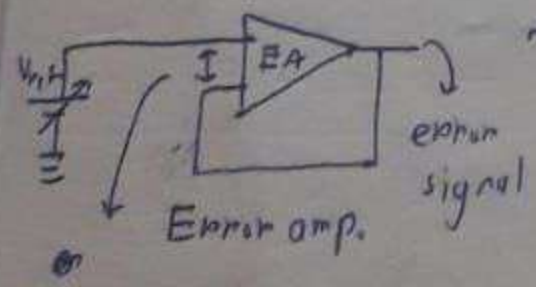
*Solution →



removal of ac gnd diff.

Used in high speed, long distance comm. [Differential signalling]

(contd.)



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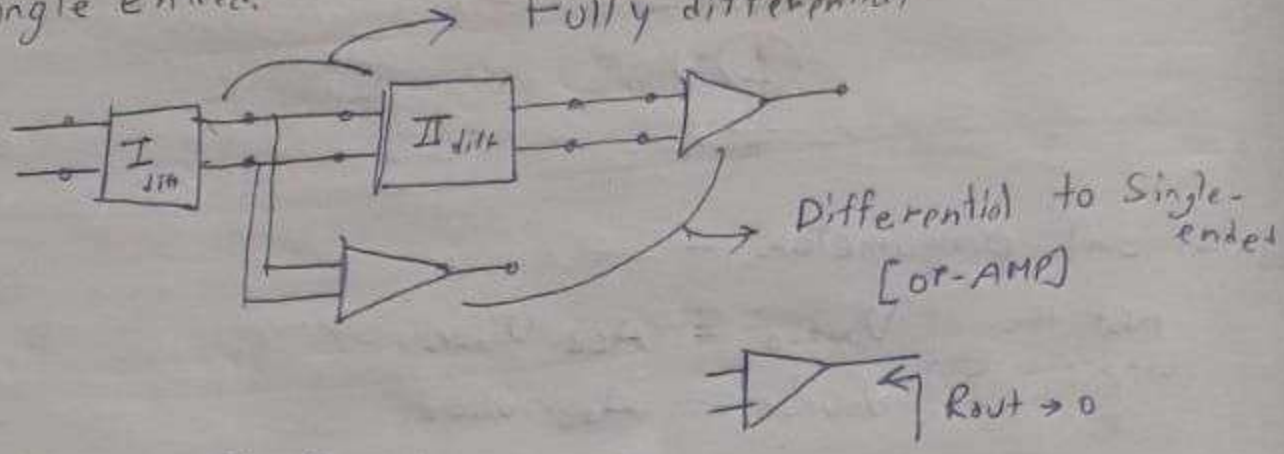
If our $V_{out-CM}$ is still larger than $V_{out-d}$, we will cascade another diff.-amp.

Finally we take differential o/p and convert it into single ended.



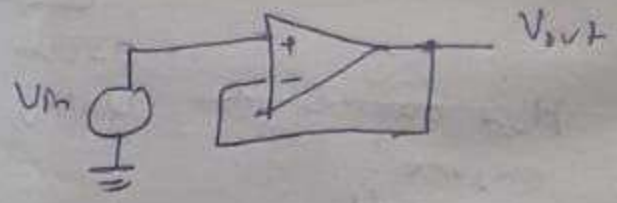

Parameters of diff. amp.-

$A_d$, $A_c$, $A_{dc}$, $A_{cd}$
Rout, Bandwidth, Signal swing ] → Small signal

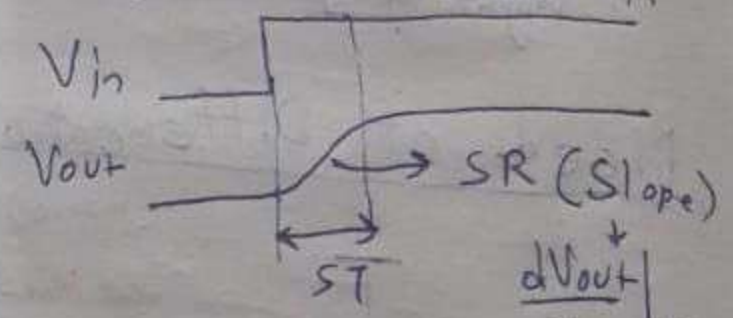
Settling time (ST)
Slew rate (SR) ] → Transient

Input Common Mode Range (ICMR) ] → Biasing

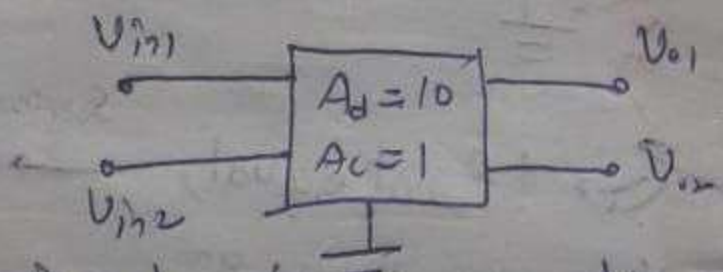
↳ Keeping all FETs in saturation.




$V_{out}$ should follow $V_{in}$




## Black-box operation of Diffamp:




I/p and o/p signals in equation form:-

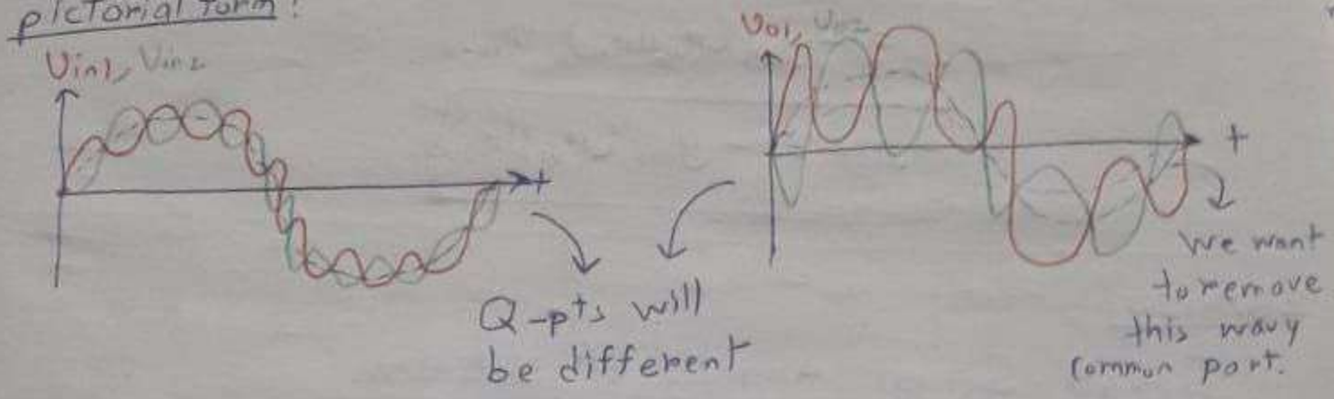
$V_{in1} = 0.5 \sin(\omega t) + 0.1 \sin(4\omega t)$

$V_{in2} = 0.5 \sin(\omega t) - 0.1 \sin(4\omega t)$

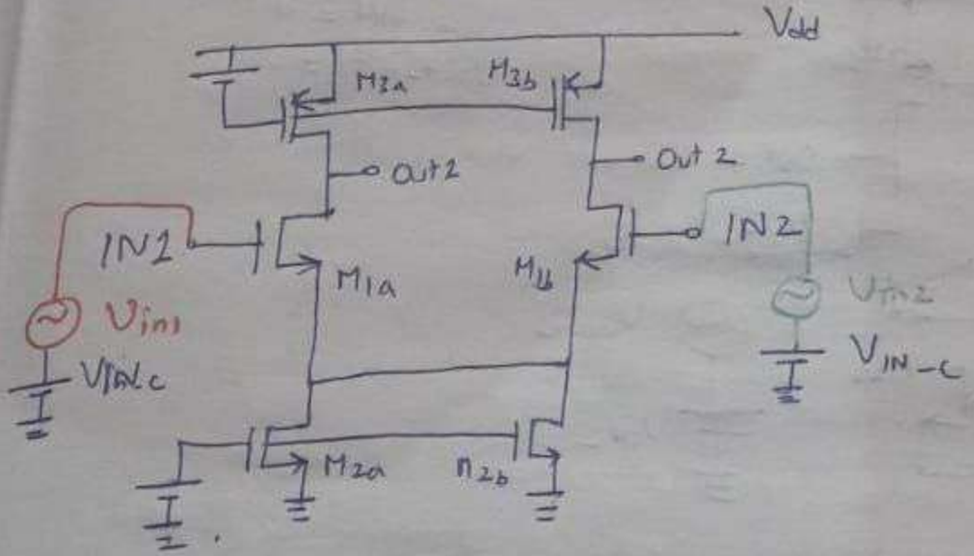
$V_{od} = 10 \times 0.2 \sin(4\omega t)$
$= 2 \sin(4\omega t)$
$V_{oc} = 1 \times 0.5 \sin(\omega t)$
$= 0.5 \sin(\omega t)$

$V_{o1} = 0.5 \sin(\omega t) + 1 \sin(4\omega t)$
$V_{o2} = 0.5 \sin(\omega t) - 1 \sin(4\omega t)$

pictorial form:

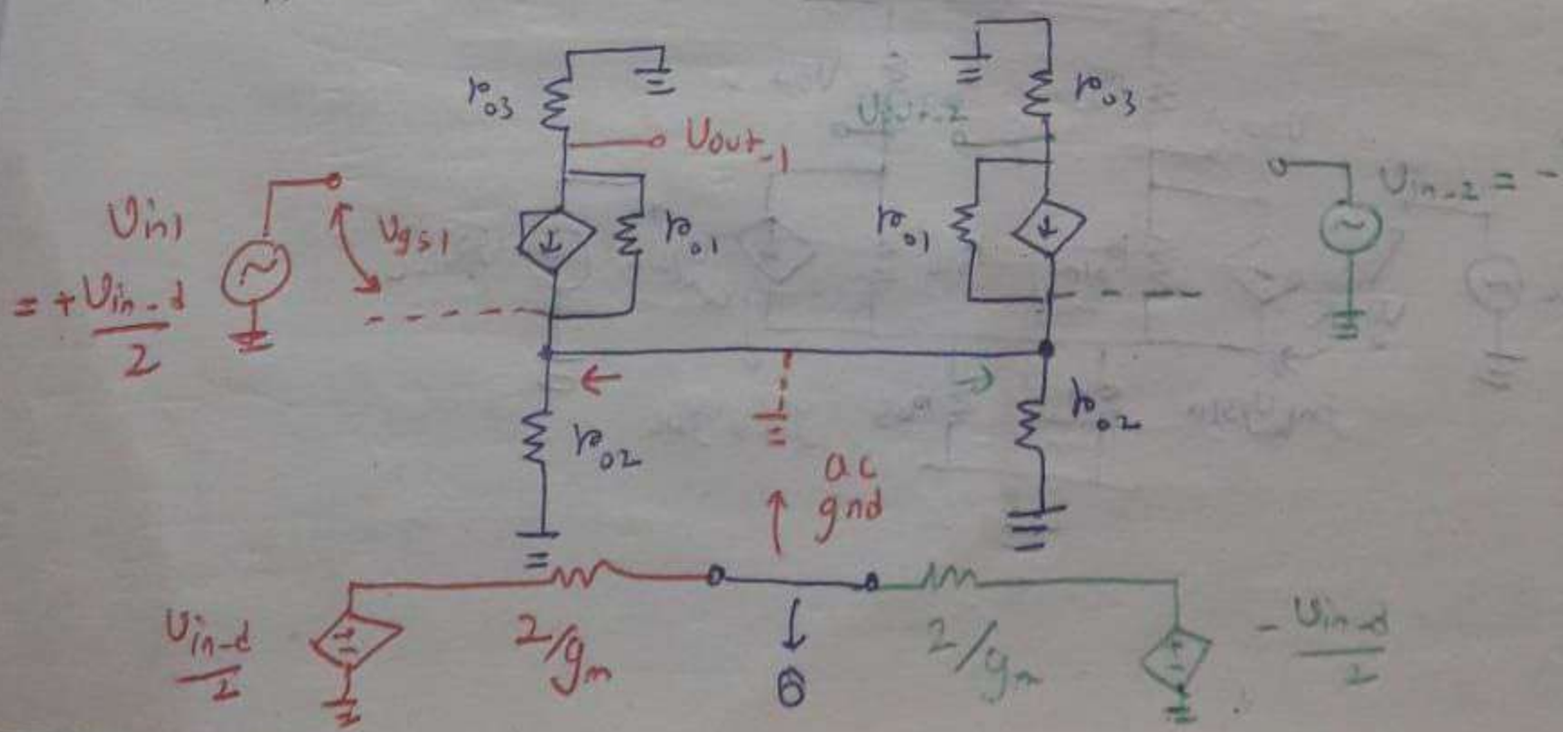



## Small Signal Equivalent circuit




$V_{in\_2} = -V_{in\_1} = \frac{-V_{in-d}}{2}$ [Differential mode]

$V_{in-c} = 0$



$$V_{out-1} = -g_{m1}(r_{o1} \| r_{o3}) \frac{v_{in-d}}{2}$$

$$V_{out-2} = -g_{m1}(r_{o1} \| r_{o3}) \left(-\frac{v_{in-d}}{2}\right)$$

$$V_{out-d} = V_{out-1} - V_{out-2}$$

$$= -g_{m1}(r_{o1} \| r_{o3})\, v_{in-d}$$

$$\boxed{A_{diff} = -g_{m1}(r_{o1} \| r_{o3})}$$

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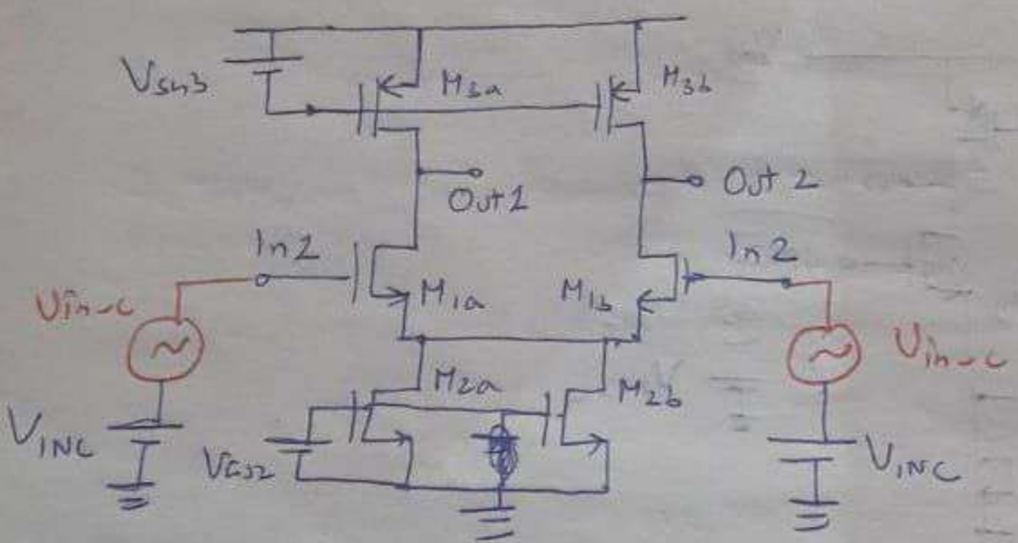
## Small Signal Analysis of Diff. Amp.

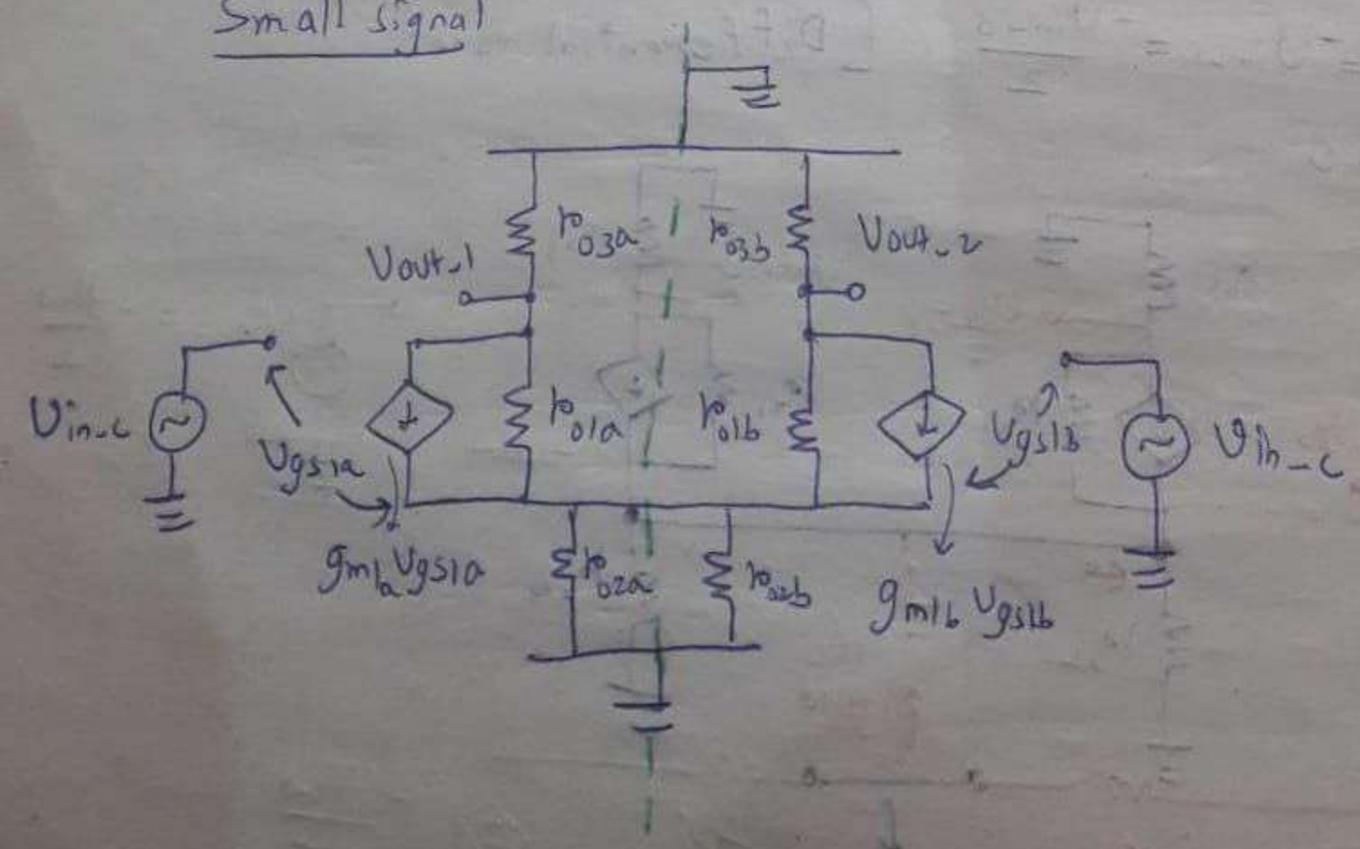
Common mode

$V_{in-diff} = 0$

$V_{out-diff} = 0$




Small signal



Since the circuit is symmetric, we can split it into 2 halves. There won't be any change.

Considering left half:

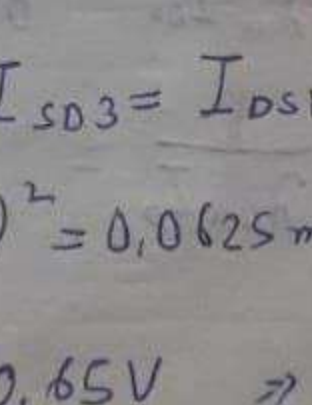
$$V_{out\_1} = -V_{in\_c} \times \frac{g_{m1a}}{1 + g_{m1a} r_{o2a}} \times r_{o3} \parallel \{r_{o1a} + r_{o2a} + g_{m1a} r_{o1a} r_{o2a}\}$$

($g_{m1a} r_{o2a}$: very high; $\{\dots\}$: very high)

$$\approx -V_{in\_c} \times \frac{r_{o3}}{r_{o2a}}$$

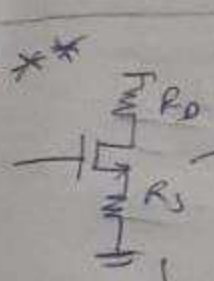
$$A_c = \frac{V_{out\_1}}{V_{in\_c}} = -\frac{r_{o3a}}{r_{o2a}}$$

Common-mode Half Ckt




$R_{out} = \{r_{o3a} \parallel (r_{o2a} + r_{o3a} + g_{m1a} r_{o2a} r_{o3a})\}$ (1)

**




$G_m = \frac{g_m}{1 + g_m R_S}$

$A_V \simeq -\frac{R_D}{R_S}$

$\hookrightarrow G_m = \frac{g_m}{1 + g_m R_S + \frac{R_S}{R_D}}$

$g_m R_S \gg \frac{R_S}{R_D}$

Hence we ignore it

## Numeric

$k_n' = 0.1 mA/V^2$ $V_{th} = 0.4V$ $W_1 = 10\mu$ $L_1 = 0.5\mu$

$k_p' = 0.04 mA/V^2$ $V_{tp} = -0.3V$ $W_3 = 25\mu$ $L_3 = 0.5\mu$

$\lambda = 0.01/L(\mu)$ $C_{ox} = 10 fF/\mu^2$ $W_2 = 20\mu$ $L_2 = 1\mu$

$C_{ov} = 0.005/\mu$

$V_{dd} = 1.8V$ $V_{GS2} = 0.65V$ $V_{SG3} = 0.55V$ $V_{G1} = 0.4V$

$\hookrightarrow V_{IN-C}$

should be in sat.

1st ensure: $I_{SD3} = I_{DS2}$

$$I_{DS2} = \frac{0.1}{2} \times \frac{20}{1} \times (0.65 - 0.4)^2$$

$$= 0.0625 mA = I_{SD3} = I_{DS1}$$

$$I_{SD3} = \frac{0.04}{2} \times \frac{25}{0.5} \times (0.55 - 0.3)^2 = 0.0625 mA$$

$$\Rightarrow V_{GS1} = V_{Tn} + \sqrt{\frac{2 I_{D1}}{K_n' (\frac{W}{L})_1}} = 0.65V \Rightarrow V_{S1} = V_{D2} = 0.9 - 0.65 = 0.25V$$

$V_{G2} - V_{tn} = 0.65 - 0.4 \leq 0.25 = V_{D2}$

Hence $M_2$ is in saturation (edge)

If $\lambda_{3a} = \lambda_{2a}$ (suppose!)

$\Rightarrow I_{D3a} = I_{D2}$

$\Rightarrow (1 + \lambda_{3a} V_{SD3}) = (1 + \lambda_{2a} V_{DS2})$

$\Rightarrow V_{SD3} = V_{DS2}$

$\Rightarrow V_{dd} - V_{out} = V_{ds2}$

$\Rightarrow V_{out} = V_{dd} - V_{ds2}$

We should use:
$\lambda_{3a} V_{SD3} = \lambda_{2a} V_{DS2}$
in general

$\Rightarrow V_{SD3a} = \frac{V_{DS2a}}{2}$

$\Rightarrow V_{out} = V_{dd} - \frac{V_{ds2}}{2}$

$= 1.8 - 0.125$

But $V_{SD3} = \frac{V_{DS2}}{2} = 0.125$

$\Rightarrow$ Transistor 3 in triode

We actually need to take

$1 + \lambda(V_{DS} - V_{D(sat)})$

$\Leftarrow$

Actually no guarantee that it will be in saturation.

$V_{out} = 1.8\,V - (V_{sd\,sat(3a)} - 0)$

$= 1.8 - 0.25$

$= 1.55\,V$

[$M_2$ in edge of sat. $\rightarrow$ Circuit can be anywhere]

This ckt. is for academic purpose. In reality it won't work while applying signal as lower half will get clipped off ($V_{in} \downarrow \Rightarrow V_{S1} = V_{G2} \downarrow \rightarrow M_2$ in triode)

$g_{m1a} = 100 \times \frac{10}{0.5} \times (0.25)\,mA/V = 0.5\,mA/V$

$\lambda_{1a} = \lambda_{3a} = 0.02\,V^{-1}$ $\quad \lambda_{2a} = 0.01\,V^{-1}$

$r_{o1a} = \frac{1}{\lambda_{1a} I_{D1}} = \frac{1}{0.02 \times \frac{1}{10}} = 800\,k\Omega = r_{o3a}$

$r_{o2a} = \frac{1}{\lambda_{2a} I_D} = 1600\,k\Omega$

$|A_d| = g_{m1}(r_{o1} \| r_{o3})$

$= 0.5 \times 400$

$= 200\ V/V$

$|A_c| = \frac{r_{o3a}}{r_{o2a}} = \frac{r_{o3b}}{r_{o2b}}$

$= 0.5\ V/V$

As $M_2$, around triode :-

$|A_d|$ doesn't involve $r_{o2}$ → No effect [Little possible $\because g_m \uparrow Z_o \downarrow$]

$|A_c|$ increases because $r_{o2}$ decreases on $M_2$ coming in triode.

We can tolerate for cases whose $V_{in-c} \approx 0$.

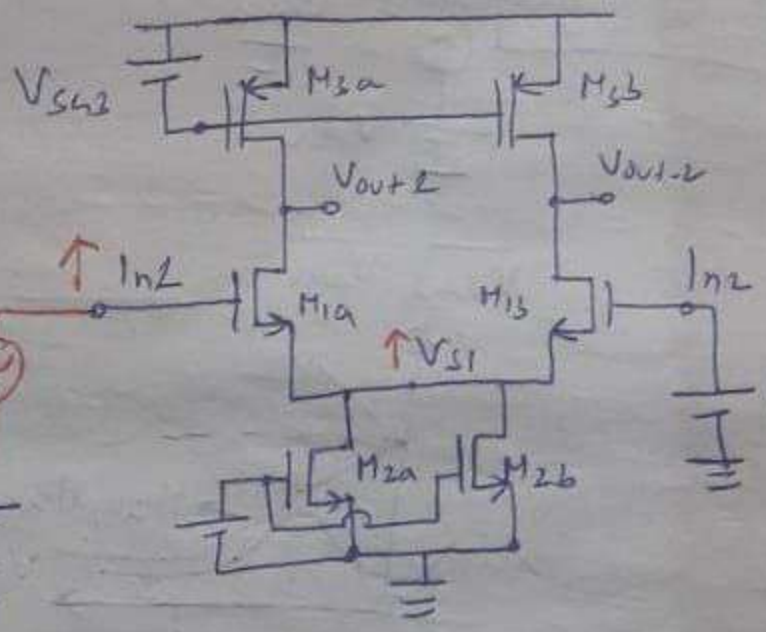
## Large Signal Analysis of Diff. Amp.

### Quasi - Diff. Input:

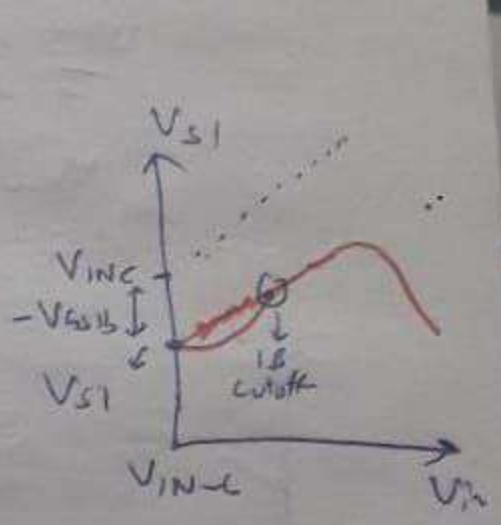
$V_{IN2} = V_{INC}$

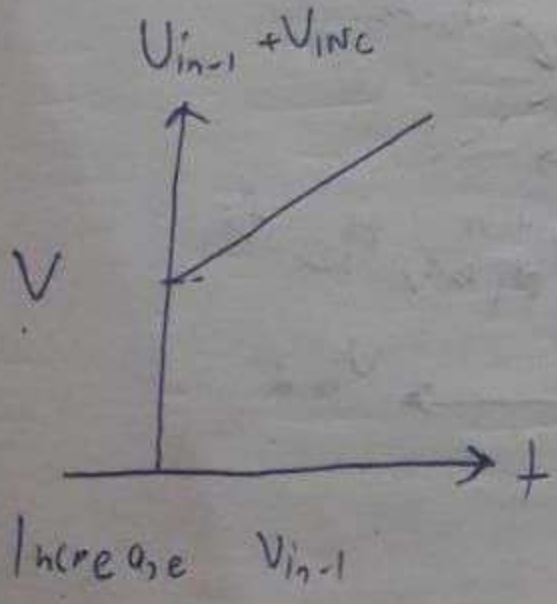
$V_{IN1} = V_{INC} + V_{in-1}$

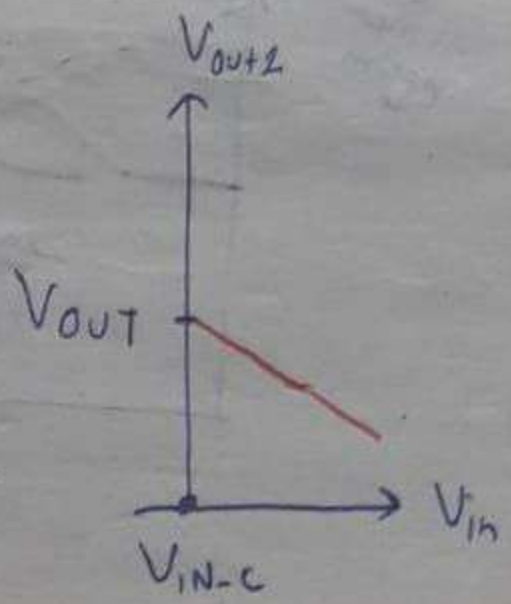
$V_{S1} = V_{INC} - V_{GS1}$

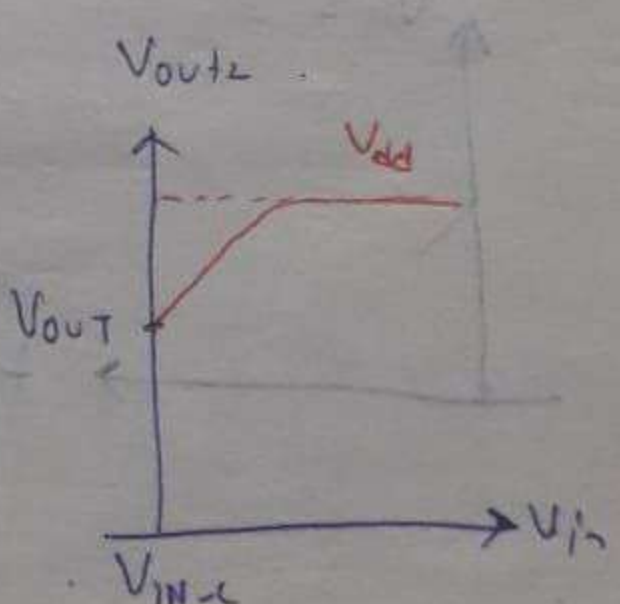



Not small Not sinusoidal



$V_{IN1} \uparrow \Rightarrow V_{S1} \uparrow$ (at lower rate)

$\downarrow$

M1b going into cutoff (no respect given)

$\downarrow$

$V_{S1}$ will follow $V_{in-1}$ (M1a) predominantly

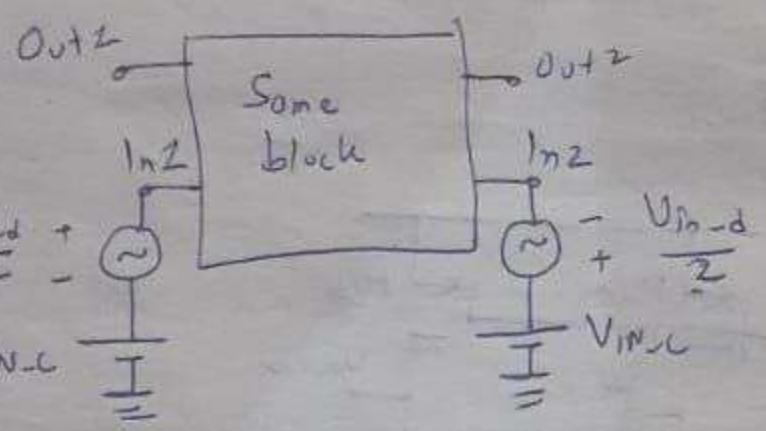
$V_{in} \uparrow \rightarrow$ I tries to increase but mismatch with current source

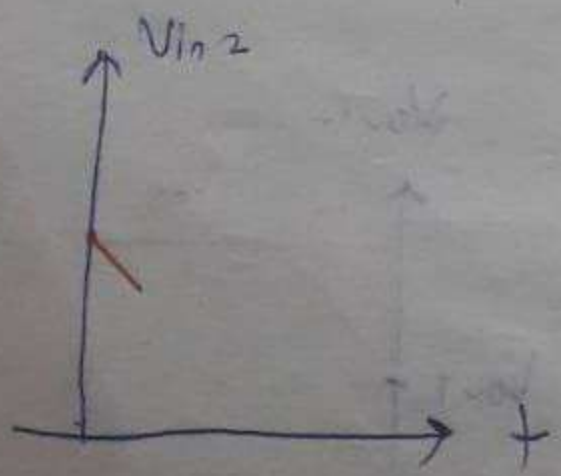
$\downarrow$

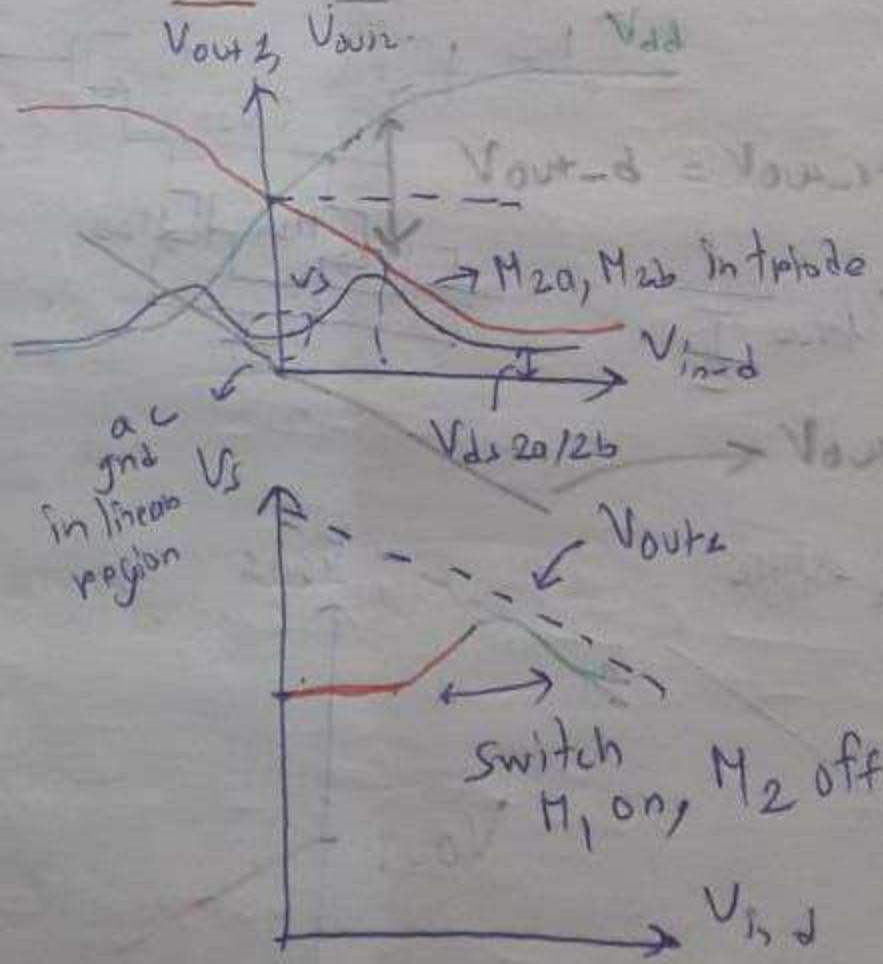
So $V_{out-2} \downarrow$

[Not able to follow → Watch video again]
[W4_Saturday - Page 3]

## Differential Input





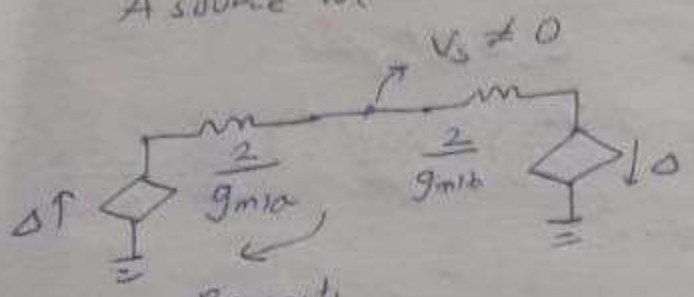



$V_s$ will tilt towards $V_{in2}$

$V_{in-d} > 0 \Rightarrow I_{ds1a} > I_{ds1b}$

$\Rightarrow g_{m1a} > g_{m1b}$

Assume we have




Respects

$\Delta \uparrow$

$\therefore \frac{2}{g_{m1a}} < \frac{2}{g_{m1b}}$

If $g_{m1a} = g_{m1b}$

$V_s \rightarrow$ virtual gnd

$V_{G1} \uparrow \Rightarrow V_{out} \downarrow$ small signal current mismatch balance

$\Rightarrow V_s \uparrow$ (Source follower towards left half)

[$V_s$ decreases because $V_{d1} = V_{out}$ decreases and $V_s$ cannot be $> V_{out}$]

$M_2$ off $\rightarrow M_1$ on

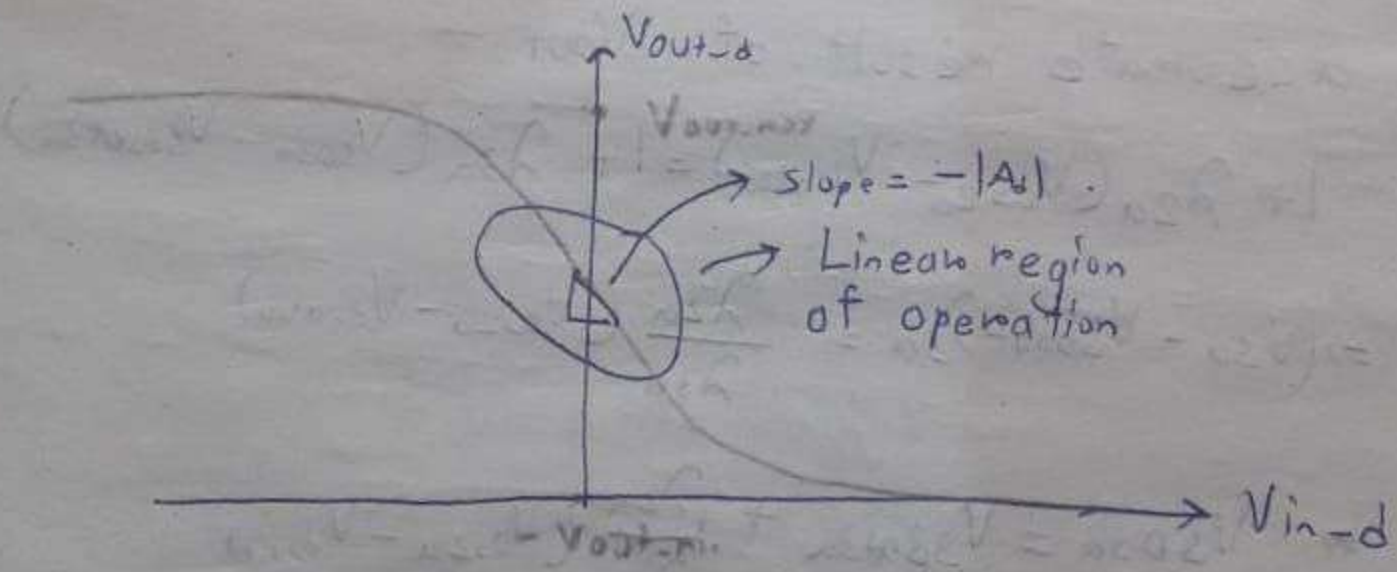
$M_{3a}$ cannot supply $M_{2a}, M_{2b}$ sum current.

Hence $M_{2a}, M_{3b}$ becomes triode so that

$I_{3a} = I_{2a} + I_{2b}$.

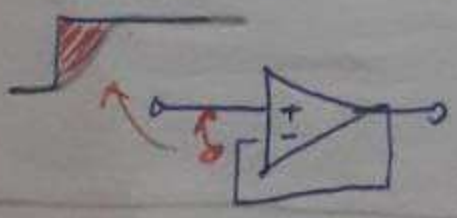
As $I_{2nd\ branch} = 0 \rightarrow Out2 = V_{DD}$

[Please watch video for this part] [W4_Saturday - Pg 6].




Transfer_characteristic

Can also be used as comparator → Extreme edges (Non-linear region)



Transient → Large signal behaviour (extreme edges)

# Week-5

## 28/9/20

Numerics:

$V_{DD} = 1.8V$

$V_{GS2} = 0.65V$

$V_{SHS} = 0.55V$

$V_{G1} = 1.1V$

$K_n' = 0.1 mA/V^2$ $V_{tn} = 0.4V$

$K_p' = 0.04 mA/V^2$ $V_{tp} = -0.3V$

$\lambda = 0.01/L(\mu m)$ $C_{ox} = 10 fF/\mu m^2$

$C_{ov} = 0.005 fF/\mu m$ $C_L = 0.5 pF$

$\left(\frac{W_1}{L_1}\right) = \frac{10\mu}{0.5\mu}$ $\left(\frac{W_2}{L_2}\right) = \frac{20\mu}{1\mu}$ $\left(\frac{W_3}{L_3}\right) = \frac{2.5\mu}{0.5\mu}$

[Same circuit of Diff. amp.]

## Output Swing

2a, 3a sizes and biases are such that 1st order currents are same

$$I_{DS2a} = I_{SD3a} = \frac{1}{16} mA \Rightarrow V_{GS1a} = V_{GS2a} = 0.65V$$

[NMOS 1, 2 → same aspect ratio]

$V_{S1} = V_{D2} = V_{G1} - V_{GS1}$

$= 1.1 - 0.65$

$= 0.45V = V_{DS2a}$

$\therefore V_{DS2a} - V_{dsat2a} = 0.45 - 0.25 = 0.2V$

For accurate result of $V_{OUT}$ →

$$1 + \lambda_{2a}(V_{DS2a} - V_{dsat2a}) = 1 + \lambda_{3a}(V_{SD3a} - V_{sdsat3a})$$

$$\Rightarrow (V_{SD} - V_{SDsat})_{3a} = \frac{\lambda_{2a}}{\lambda_{3a}}(V_{DS2a} - V_{dsat2a})$$

$$\Rightarrow V_{SD3a} = V_{sdsat3a} + \frac{\lambda_{2a}}{\lambda_{3a}}(V_{DS2a} - V_{dsat2a})$$

$$= 0.25 + \frac{0.5}{1} \times 0.2$$

$$= 0.35V$$

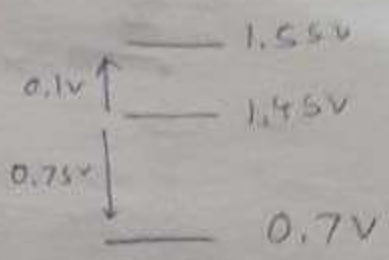
$\therefore V_{OUT} = V_{DD} - V_{SD3A} = 1.8 - 0.35 = 1.45V$

$M_3$ in sat → $V_{SD3} \geq V_{SG3} - |V_{TP}|$

$\Rightarrow 1.8 - V_{D3} \geq 0.55 - 0.3$

$\Rightarrow V_{D3} \geq 1.55V$

$V_{out\_max} = 1.55V$




$M_1$ in sat → $V_{GS1} - V_{TN} \leq V_{DS1}$

$\Rightarrow V_{G1} - V_{TN} \leq V_{D1}$

$\Rightarrow V_{D1} \geq 1.1 - 0.4 = 0.7$

$V_{out\_min} = 0.7V$

$V_{Outswing} = 1.55 - 0.7 = 0.85V$ [PP swing]

## Input Common Mode Range

Lower limit:

$M_2$ in saturation →

$V_{IN\_C} - V_{GS1A} = V_{dsat\_2A}$ [Don't do $V_{GS1} > V_{TN}$ as $V_{GS}$ is fixed in sat.]

- for fixed current

↓

You did this mistake in assignment [DONT REPEAT]

$V_{GS}$ is fixed ∵ $I_{DS}$ is fixed.

$V_{IN\_C}|_L = V_{GS1A} + V_{dsat\_2A}$

$= 0.65 + 0.25$

$= 0.9V$

Upper limit:- $M_1$ in saturation:

$V_{OUT} = V_{IN\_C}|_U - V_{TH}$

$\Rightarrow V_{IN\_C}|_U = V_{OUT}|_U + V_{TH}$

$= 1.45 + 0.4$

$= 1.85 \rightarrow$ (Exceeds $V_{DD}$)

$= V_{DD} - V_{Sdsat\_3A} + V_{TH}$

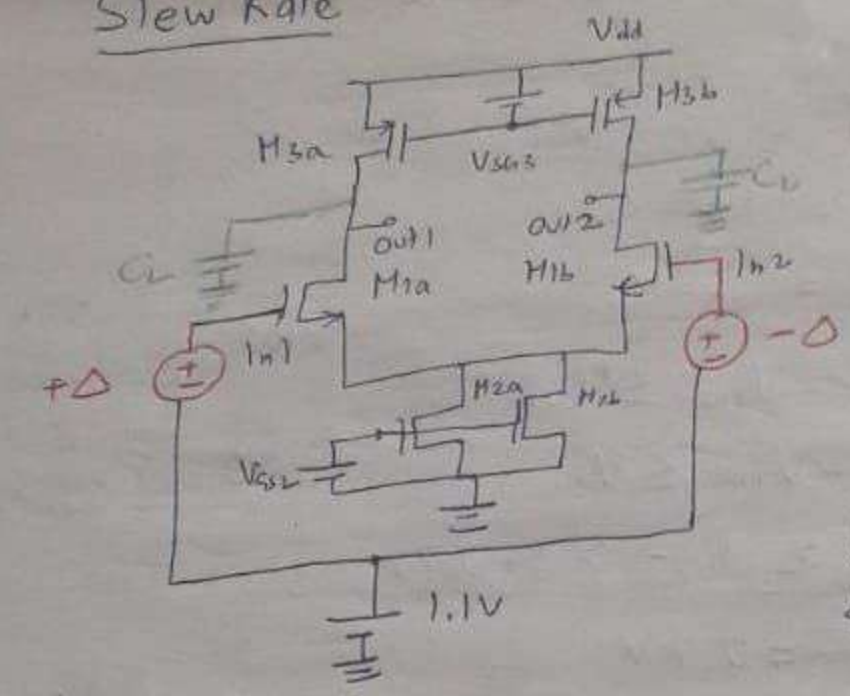
$= 1.8 - 0.25 + 0.4$

$= 1.95V$ (Aggressive)

$V_{in}$ - Swing $= 1.95 - 0.9 = 1.05V$ [PP swing]

# Slew Rate

$C_L = 0.5pF$




$\Delta = 0$ : $I_{ds} = \frac{1}{16}mA$

$V_{out} = 1.45V$

$\Delta > 0$ Sufficiently large

1a → On [$V_{GS} > 0$]

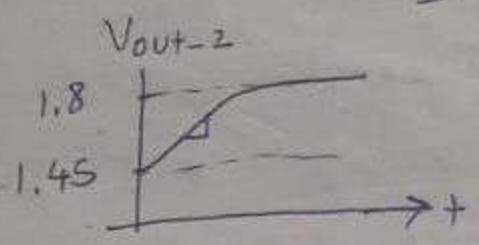
1b → Off [$V_{GS} < 0$]

As 1b is off, current from 3b flows into capacitor

As 1a is off, and $M_{2a}$, $M_{2b}$ demand twice current initially, and 3a alone cannot give it; so $C_L$ at $V_{out-2}$ discharges to give another component of $I_D$.

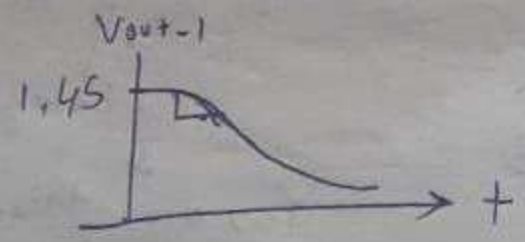
↓

After some time 2a, 2b falls into triode so that it fulfills $M_{3a}$ current. ∴



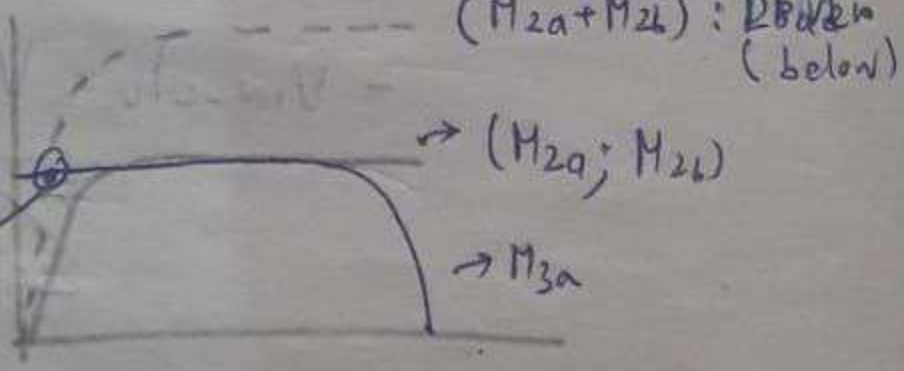

$$I_{SD3} = C_L \frac{dV_{out2}}{dt}$$

$$\frac{dV_{out2}}{dt} = \frac{I_{SD3}}{C_L} = \frac{1}{16} \times 10^{-3} \times \frac{10^{12}}{0.5} = \frac{1}{8} V/ns$$




$$I_{DS1} = -C_L \frac{dV_{out1}}{dt} \Rightarrow \frac{dV_{out1}}{dt} = -\frac{I_{DS1}}{C_L} = \frac{-1}{16} \times 10^{-3} \times \frac{10^{12}}{0.5} = \frac{1}{8} V/ns$$

$$\text{Slew rate} = \frac{d}{dt}(V_{out2} - V_{out2}) = \frac{1}{4} V/ns = 0.25 V/ns$$




Thus $M_{3a}$ drives $M_{2a}$, $M_{2b}$ into triode

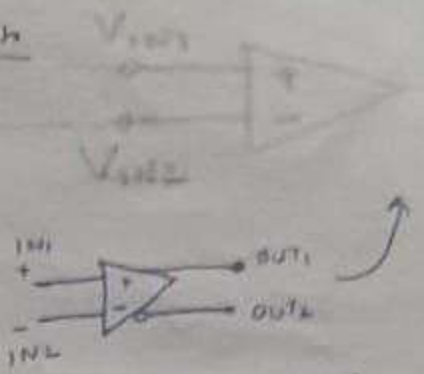
Assignment-4

29/9/20 [Tuesday → WS]

## Differential to Single Ended Amplifier

- Topology and operating point: [Video]

[Watch video for step by step analysis]

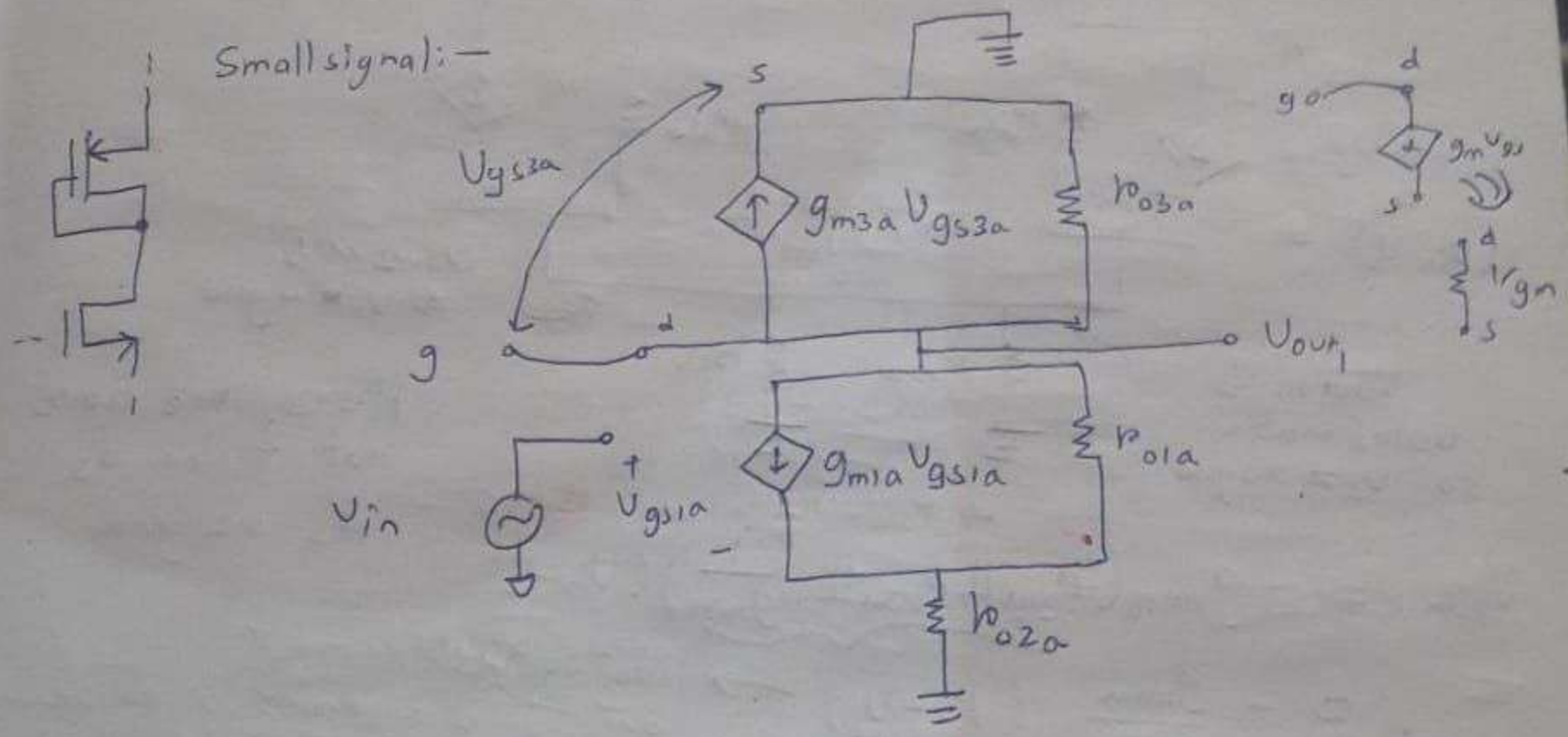



One way →
1) Take out only $out_2$ and declare as $V_{out}$

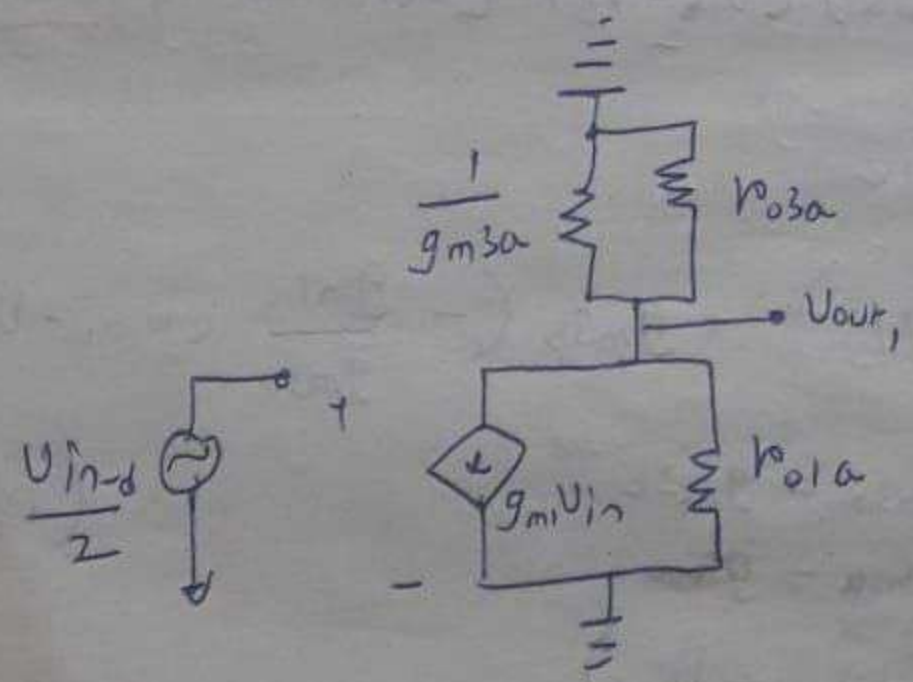
Making $M_{3a}$ → diode connected

Signal strength at out1 reduces ⇓ Issue: Gain = $\frac{A_{diff}}{2}$

Small signal:-




Diff mode only ⇓



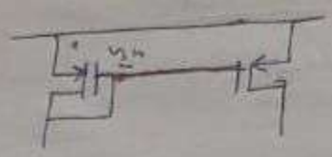

$$V_{out_1} = -\frac{V_{in-d}}{2} g_{m1a} (r_{o1a} \| r_{o3a} \| \frac{1}{g_{m3a}})$$

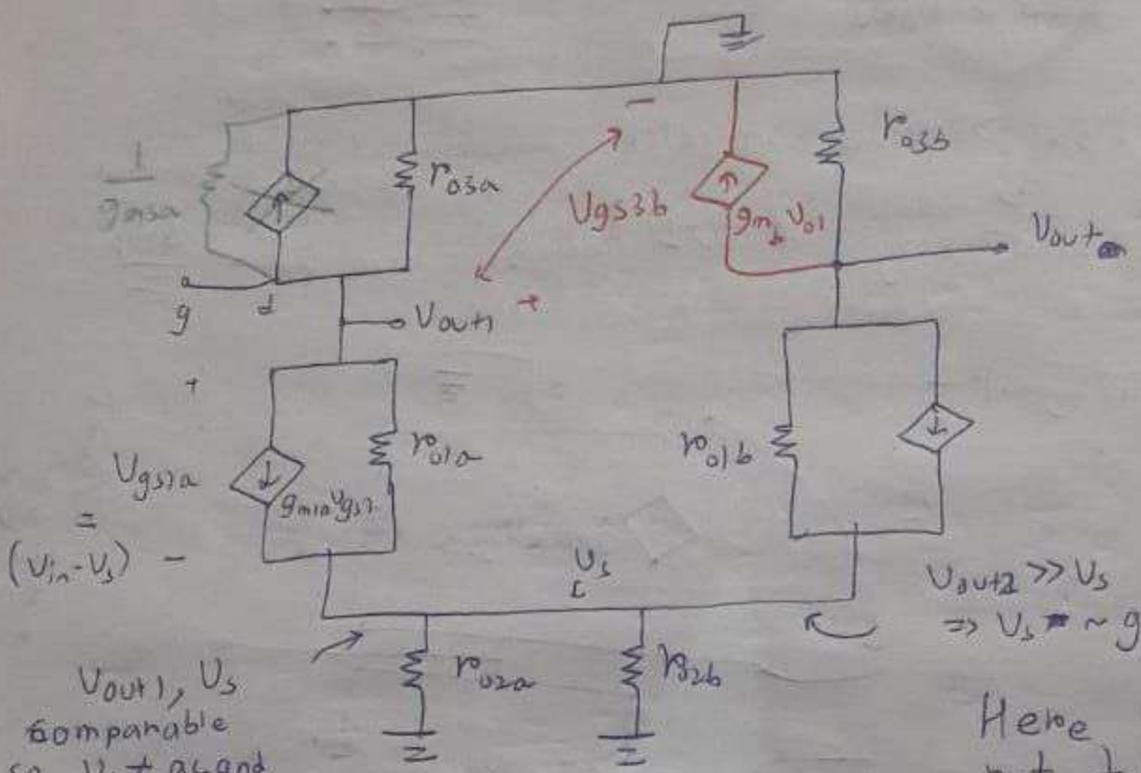
$$\simeq -\frac{V_{in-d}}{2} \left(\frac{g_{m1a}}{g_{m3a}}\right)$$

We have hampered the signal at out 1 only,

Another change:- [Video]

We connect $V_{out1}$ to gate of $M_{3b}$.






$= (V_{in} - V_s)$ −

$V_{out2} \gg V_s$
$\Rightarrow V_s \neq$ ~ gnd

$V_{out1}$, $V_s$ comparable so $V_s \neq$ ac gnd

Here we have not taken $V_s$ as ac gnd.

$\rightarrow r_{o1a} + r_{o2} \| r_{o3a} + g_{m1a} r_{o1a} r_{o2} \| r_{o3b}$

$$V_{out1} = -g_{m1a}\left(r_{o1a} \| r_{o3a} \| \frac{1}{g_{m3a}}\right)(V_{in} - V_s)$$

$$\simeq -\frac{g_{m1a}}{g_{m3a}}(V_{in} - V_s)$$

↳ Not completely correct but $\frac{1}{g_{ms}}$ is dominating so no problem (i.e. $r_{o1a}$ is not connected to gnd)

$$V_{out} = -g_{m1b}(r_{o3b} \| r_{o1b})(V_{in_2} - V_s) \quad \text{[Before making change]}$$

After making change

$$V_{out} = \left[g_{m1b}(V_{in2} - V_s) + g_{m3b}\left(-\frac{g_{m1a}}{g_{m3a}}(V_{in1} - V_s)\right)\right] (r_{o1b} \| r_{o3b})$$

$g_{m3a} = g_{m3b}$

$g_{m1a} = g_{m1b}$

$$= -g_{m1}(r_{o1} \| r_{o3})(V_{in2} - V_{in1})$$

$$\boxed{\frac{V_{out}}{V_{in2} - V_{in1}} = -g_{m1}(r_{o1} \| r_{o3})}$$

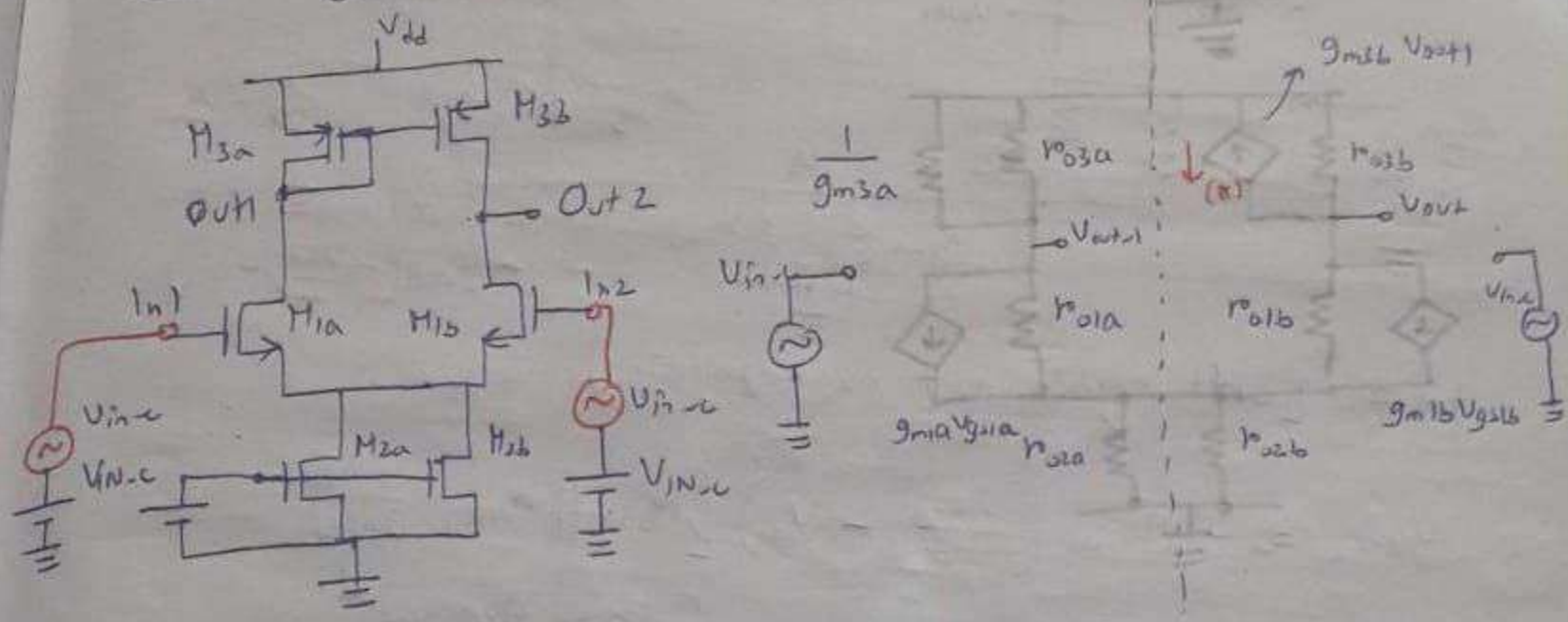
$V_s \ll V_{out}$

$$\boxed{A_d = g_{m1}(r_{o1} \| r_{o3})}$$

Advantages of doing the connection -

1) No need of $V_{GS3}$ for $M_{3a}$, $M_{3b}$
2) $V_{out-2}$ obtains the entire differential ~~gain~~ gain.
3) Common mode gain advantage.

## Small Signal Analysis for Common Mode [Video]




$$V_{out-1} = -\frac{g_{m1a}}{g_{m3a}} V_{in}$$

$$g_{m3b} \times V_{out1} = -\cancel{g_{m3b}} \times \left(\frac{1}{\cancel{g_{m3a}}} \times g_{m1a} V_{gs}^2\right)$$

$$= -g_{m1a} V_{gs1a} \quad (*)$$

This approx. if not true would make vout dependent on $V_S$ ∴ $\rightarrow g_{m1b} V_{gs1b}$ → The current is helping each other by not flowing into $r_{o3b}$, $r_{o1b}$ [without disturbing $V_{out}$]

An implication of common mode stimulus.

$V_{out} = V_{out-1}$

Left half branch.

$$V_{out-1} = -V_{in-c} \cdot \frac{g_{m1a}}{1 + g_{m1a} r_{o2a}} \cdot \left(r_{o3a} \| \frac{1}{g_{m3a}}\right)$$

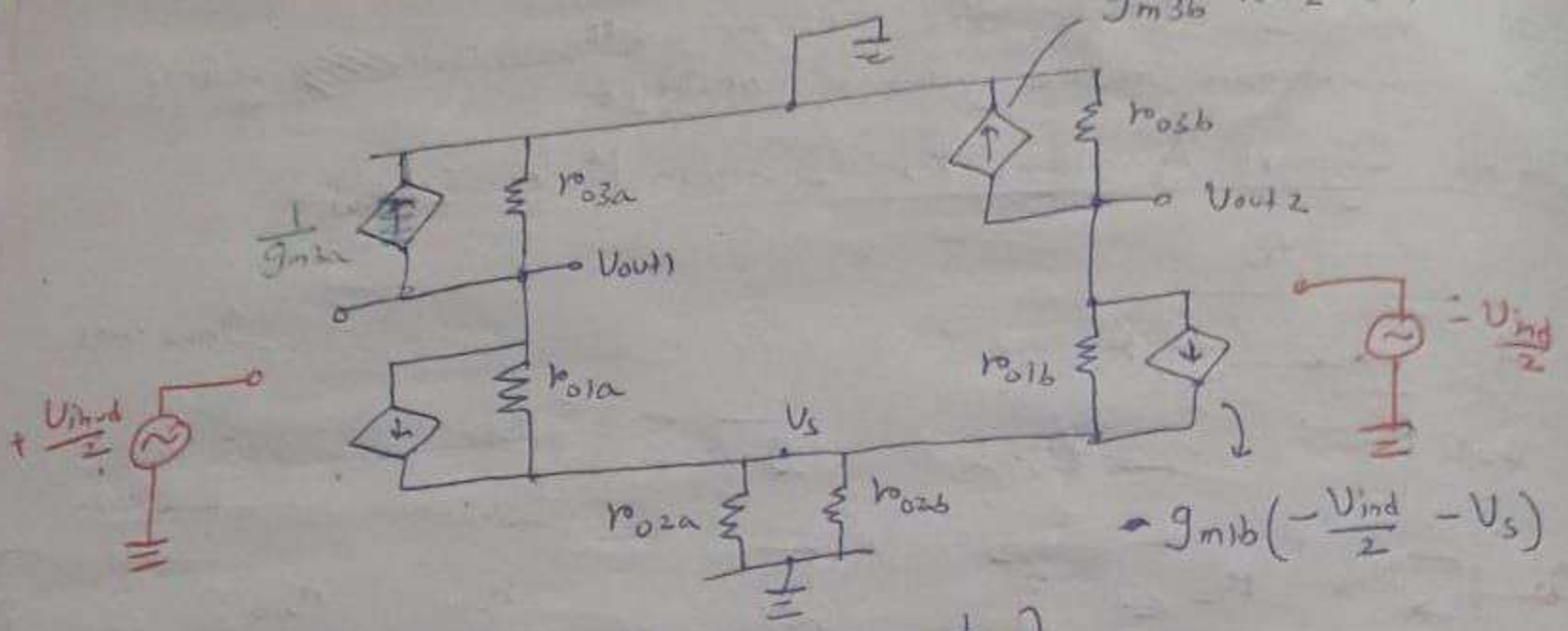
$$V_{out-1} = -V_{in-c} \cdot \frac{1}{g_{m3a} r_{o2a}}$$

More clear picture in Large Signal Analysis (Common Mode)

$$\therefore V_{out} = V_{out-1} = -\frac{1}{g_{m3a} r_{o2a}} \cdot V_{in-c}$$

$$\boxed{A_c = -\frac{1}{g_{m3a} r_{o2a}}} \rightarrow -\frac{1}{2 g_{m3} r_{o2}}$$

# Small signal (Differential mode) [Video]




$V_s \neq 0$ [Left, right half non-symmetric]

$$V_{out_1} = -g_{m1a}\left(\frac{V_{in-d}}{2} - V_s\right)\left[r_{o3a} \,||\, r_{o1a} \,||\, \frac{1}{g_{m3a}}\right]$$

[Approx.]

$$= -\frac{g_{m1a}}{g_{m3a}}\left(\frac{V_{in-d}}{2} - V_s\right)$$

$g_{m3a} = g_{m3b}$

(*) $g_{m3b}\,V_{out} = -\frac{g_{m1a}}{g_{m3a}} \cdot g_{m3b}\left(\frac{V_{in-d}}{2} - V_s\right) V_{out}$

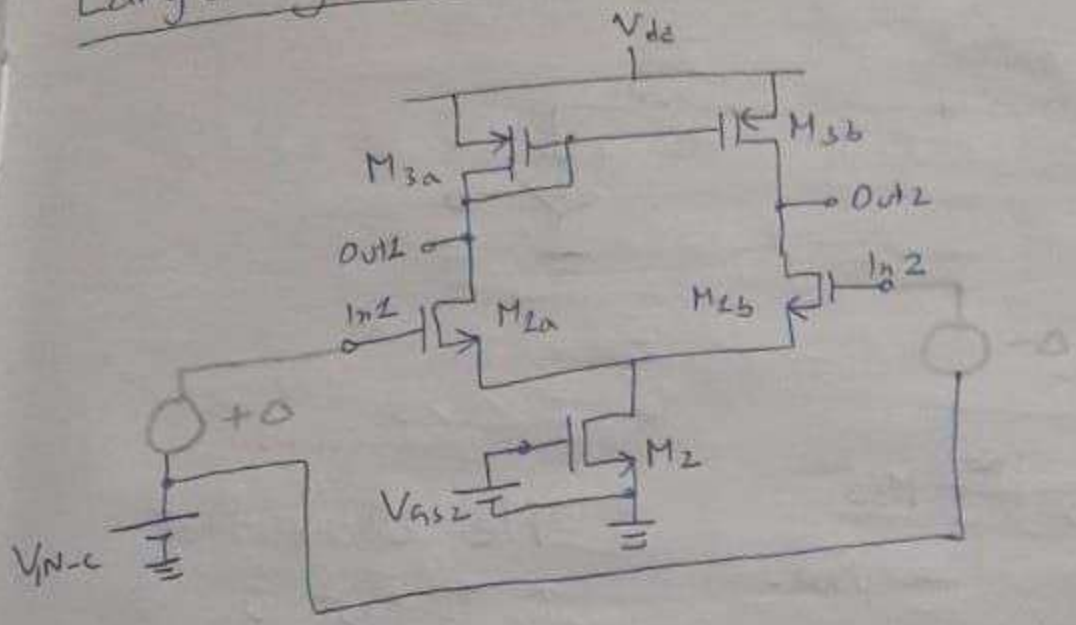
$$\therefore V_{out} = -\left[g_{m1b}\left(-\frac{V_{ind}}{2} - V_s\right) - g_{m1a}\left(\frac{V_{ind}}{2} - V_s\right)\right] \times (r_{o3b} \,||\, r_{o1b})$$

$g_{m1a} = g_{m1b}$

$$= g_{m1} V_{ind} (r_{o1b} || r_{o3b})$$

$$\therefore \boxed{\frac{V_{out}}{V_{in}} = g_{m1}(r_{o1b} || r_{o3b})}$$

## Large signal analysis (Video)




$\Delta = 0$ : $V_{OUT2} = V_{dd} - V_{sg3a}$

$$\frac{I_{DS2}}{2} = I_{SD3a} = \frac{K_p'}{2}\frac{W_{3a}}{L_{3a}}(V_{sg3a} - |V_{thp}|)^2$$

$$V_{sg3a} = |V_{thp}| + \sqrt{\frac{I_{DS2}\, L_{3a}}{K_p' W_{3a}}}$$

Say $V_{OUT2} > V_{OUT1}$

$\Rightarrow V_{DS1a} < V_{DS1b}$ ; $V_{SD3a} > V_{SD3b}$

$I_{DS1b} > I_{DS1a}$ [$\because I \propto (1+\lambda V_{DS})$]

$I_{SD3a} > I_{SD3b}$

But $I_{DS1a} = I_{S3a}$

$\Rightarrow I_{DS1b} > I_{SD3b}$ [Not possible]

$\therefore V_{OUT2} > V_{OUT1}$ (Not possible)

Similarly $V_{OUT2} < V_{OUT1}$ (Not possible)

Hence $\boxed{V_{OUT1} = V_{OUT2}} = V_{DD} - |V_{thp}| - \sqrt{\frac{I_{DS2}\, L_{3a}}{K_p' W_{3a}}}$

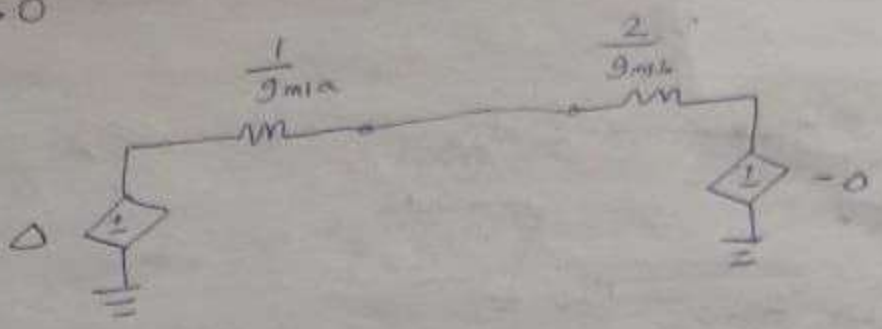
DC ↖ * Valid for $V_{in-d} = 0$

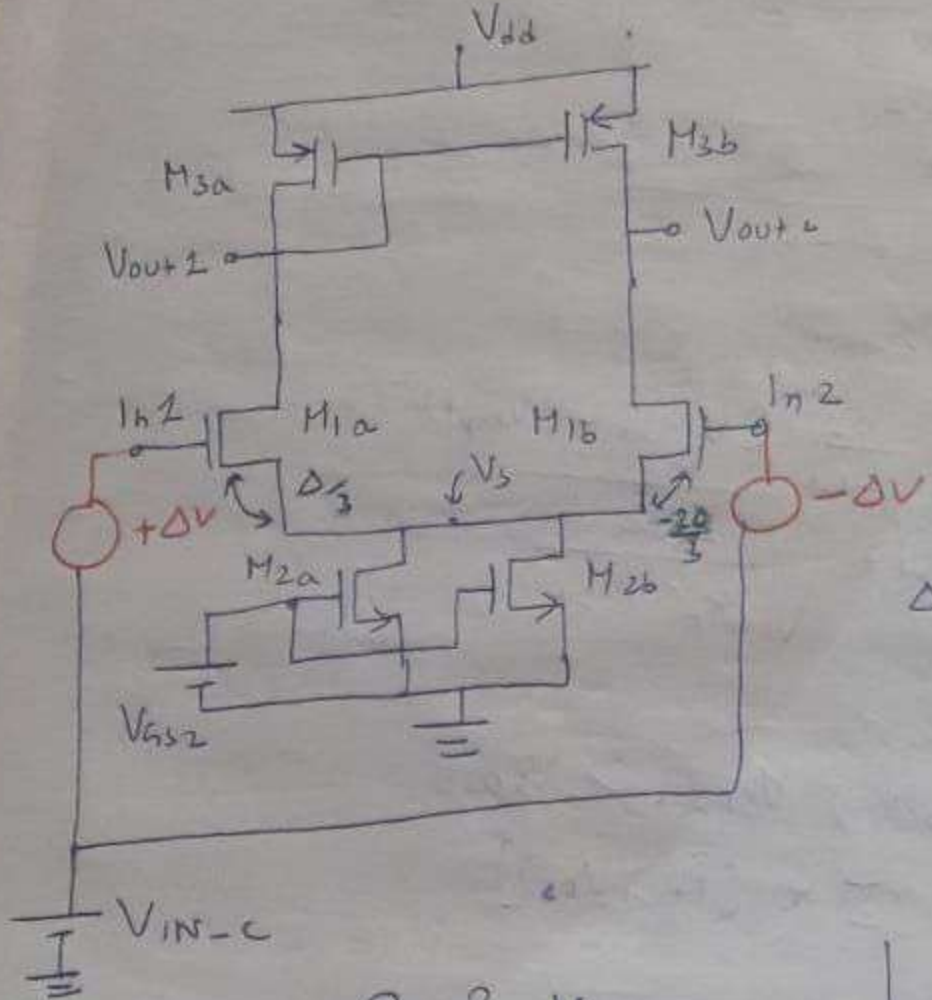
[True for CM only] [Low freq.]

AC ↙ $\boxed{V_{out1} = V_{out2}}$

3rd advantage → Common gate connection reduces gain / common mode gain.

$\Delta > 0$

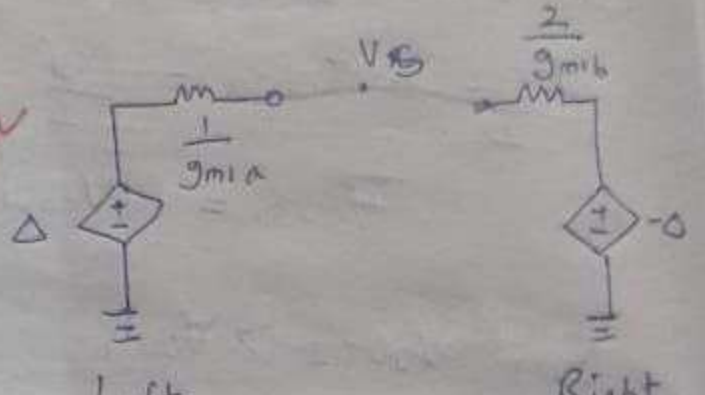



$\Delta > 0$

We claim that $V_S$ is not 0.

Reason:




$$V_S = \frac{\frac{2}{g_m}}{\frac{1}{g_m}+\frac{2}{g_m}}(2\Delta) - \Delta$$

or

$$\Rightarrow \frac{\Delta - V_S}{\frac{1}{g_m}} = \frac{V_S + \Delta}{\frac{2}{g_m}}$$

$$\Rightarrow \frac{\Delta}{2} = \frac{3V_S}{2}$$

$$\Rightarrow V_S = \frac{\Delta}{3}$$

($V_S$ tilts to left half)

$\frac{2}{g_{m1b}}$ ? How ↓

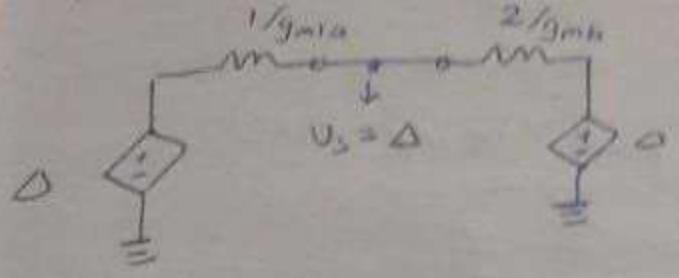
Use $\left(\frac{R_D + r_o}{1 + g_m r_o}\right)$

Left half $\rightarrow \frac{\frac{1}{g_m} + r_{o1}}{1 + g_m r_{o1}} \simeq \frac{r_o}{g_{m1} r_o} = \frac{1}{g_{m1a}}$

Right half $\rightarrow \frac{r_{o2} + r_{o1a}}{1 + g_{m1b} r_{o1}} \simeq \frac{2}{g_{m1b}}$

The Thevenin equivalents are for circuit from source side b4 connecting $S_1$, $S_2$.

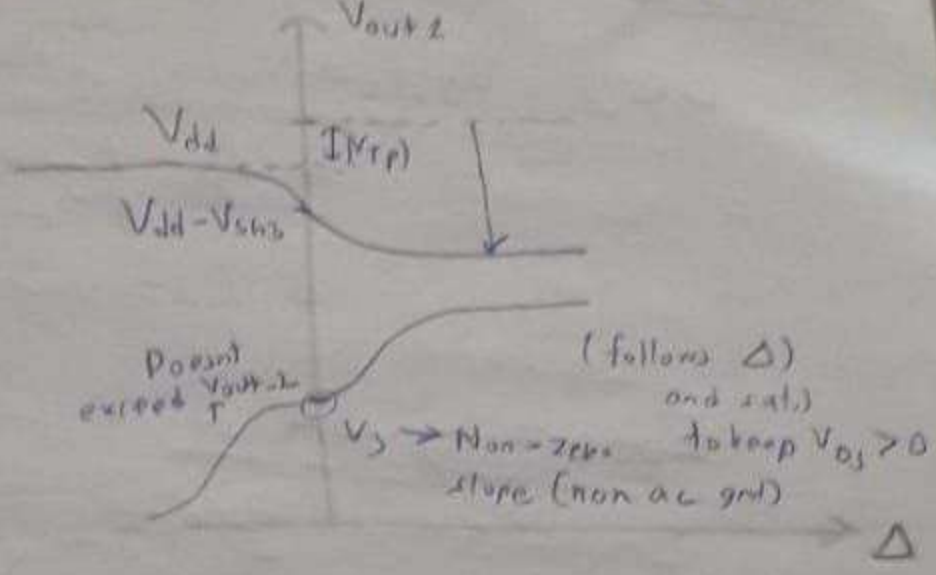
Consider now common mode




Due to loading by $M_{2a}$, $M_{2b}$ →
$V_S$ is a little less than Δ

Hence for both diff. and common mode;
$V_S$ is not-ac gnd.

Considering diff. voltage we observe $V_{out1}$



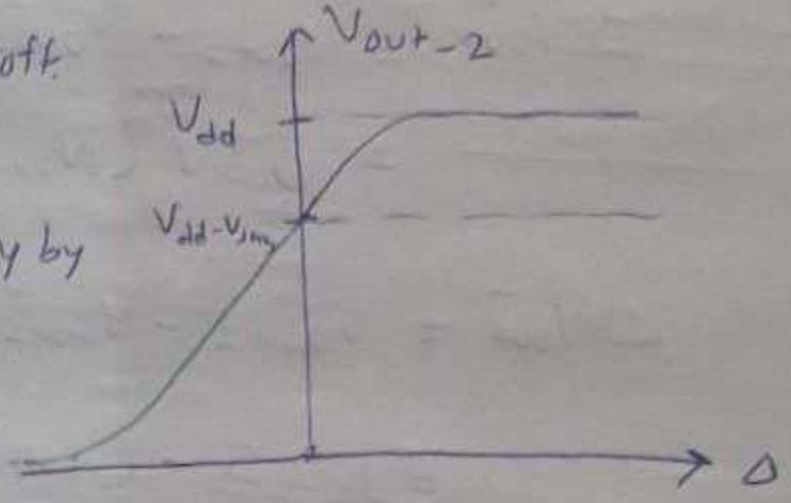

$I_{SD3} \uparrow \Rightarrow V_{SD} \uparrow \Rightarrow V_{out1} \downarrow$

Saturates and supports $I_{2a}$, $I_{2b}$.

Now see $V_{out-2}$

$M_{3b}$ stays on but $M_{1b}$ becomes off
↓
[∵ $V_{sg3b} = V_{sg3a}$]

And current is supported only by left branch $M_{3a}$, $M_{1a}$. Thus to make current in $M_{3b} = 0$;
$V_{out2} = V_{DD}$.




Now Let's make Δ<0

⇒ $M_{1a}$ becomes off [$V_{sg3} \rightarrow |V_{Tp}|$]

⇒ $M_{1b}$ is on strongly → Drives itself and $M_{2a}$, $M_{2b}$ into triode to help current supply.

Assignment-5
(Sunday Midnight)

1/10/20

Numeric

In DC, $V_{OUT2} = V_{OUT1}$ [As per theory - cut-off]

$= V_{dd} - V_{sg3a}$

$= V_{dd} - \sqrt{\frac{I_{DS2}}{K_p'\left(\frac{W}{L}\right)_3}} - |V_{TP}|$ $I_{SD3} = \frac{1}{2} I_{DS2}$

$I_{DS2} = \frac{1}{8}$ mA

$= 1.8 - \sqrt{\frac{\frac{1}{8}}{0.01 \times \frac{25}{0.5}}} - |V_{TP}|$

$= 1.8 - 0.3 = 1.25V$

~~$= 1.671V$~~ ~~$- 0.3$~~

~~$= 1.371V$~~

$V_{OUT} = 1.25V$

$\Delta V_{out}^{+} = V_{out2}|_{max} - V_{OUT2}$

$= 0.3V\ (|V_{tp}|)$

$V_{out2\,max} = V_{DD} - V_{dsat-3b}$

$V_{out2} = V_{DD} - V_{dsat3b} - |V_{tp}|$

$\Delta V_{out}^{-} = V_{OUT2} - V_{out2}|_{min}$

$= 1.25 - (1 - 0.4)$

$= 0.65V$

$V_{out2\,min} = V_{G1} - V_{Tn}$

$\hookrightarrow OS = 0.3 + 0.65 = 0.95V$

Slew rate (SR+) $= \frac{I_{CL}}{C_L} = \frac{10^{-3}}{8} \times \frac{10^{9}}{0.5} = \frac{10^{9}}{4}$

$= 0.25$ V/ns

$V_{in2}$ ↓ such that $I_{DS3b} = I_{CL}$

By current mirror:

As $I_{3a}$ is $\frac{1}{8}$ mA $\Rightarrow I_{52} = \frac{1}{8}$ mA ↴

Unlike fully diff. amp.; due to fixed $V_{SG}$; $I_{CL} = \frac{1}{16}$ mA

$$= \frac{I_{CL}}{C_L} = \frac{10^{-3}}{8} \times \frac{10^{12}}{0.5}$$

$$= 0.25 \text{ V/ns}$$

SR⁻

$M_{1a}$ off ($M_{3a,3b}$ off)

$M_{1b}$ on $\rightarrow I_{DS2} = I_{CL} = \frac{1}{8}$ mA

(full current)

ICMR: $V_{IN-C}$ (variable)

We consider $I_{DS2} = \frac{1}{8}$ mA (constant)

$\Rightarrow I_{SD3a} = \frac{1}{2} \times \frac{1}{8} = \frac{1}{10}$ mA

$\therefore V_{SG3a} = V_{SG3b} = 0.55$ V

$V_{out_1} = 1.25$ (As said earlier)

$S_2$

$V_2(t)$

$$V^+_{INLC\,max} = V_{OUT-1} + V_{Tn} \quad (M_1 \text{ in sat.})$$

$$= V_{dd} - V_{SG3a} + V_{TN}$$

$$= 1.25 + 0.4$$

$$= 1.65 \text{ V}$$

[Both side $V_{OUT}$ are same so right side also similar]

$$V^-_{IN-C\,min} = V_{GS1a} + V_{dsat2} \quad (M_2 \text{ in sat})$$

$$= 0.65 + (0.65 - 0.4)$$

$$= 0.9 \text{ V}$$

ICMR has reduced compared to previous case because $V^+_{IN-C}$ was greater than $V_{DD}$ earlier

$R_{out} = r_{o1b} \,||\, r_{o3b}$ $(V_s \ll V_{out})$ $r_{o1b} = \frac{1}{\frac{0.01}{0.5} \times \frac{1}{16}} = 800\text{k}\Omega$

$= \frac{800}{2} = 400\text{k}\Omega$ $r_{o3b} = \frac{1}{\frac{0.01}{0.5} \times \frac{1}{16}} = 800\text{k}\Omega$

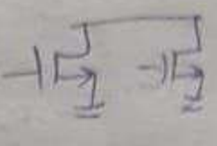
$$B.W. = \frac{1}{R_{out} C_L} = \frac{1}{4\times10^5 \times 0.5\times10^{-12}} = \frac{2}{2}\times10^7$$
$$= 5\ Mrad/s$$

[$V_{GS}$ → within ICMR]

$$A_d = g_{m1} R_{out} \qquad g_{m1a} = \sqrt{2 I_{DS1} K_n' \left(\frac{W}{L}\right)_1}$$
$$= 0.5\ mA/V$$

$$= 200 V/V$$

$$A_c = \frac{-1}{g_{m3a} r_{o2a}} = -\frac{1}{2 g_{m3} r_{o2}}$$



$$\left[\frac{g_{m1a}}{1+2 r_{o2} g_{m1a}} \times \frac{1}{g_{m3a}}\right] \qquad r_{o2} = \frac{8\times10^3}{0.01} = 800k\Omega$$

$$= -\frac{1}{800}\ V/V$$

3/10/20

Numeric

Same parameters

→ $W_{1a} = 10.1\ \mu m$ (±1% deviation)

→ $W_{1b} = 9.9\ \mu m$

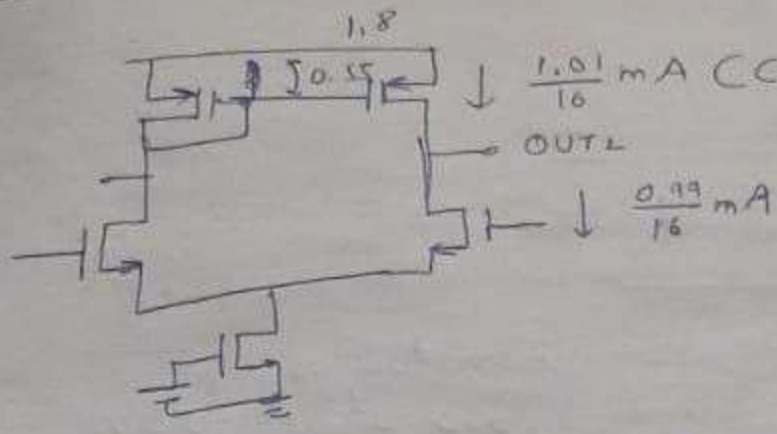
$$I_{DS1a} + I_{DS1b} = \frac{1}{8} mA \qquad [V_{GS1a} = V_{GS1b}]$$

$$\frac{I_{DS1a}}{I_{DS1b}} = \frac{K_n' \frac{W_{1a}}{2L_{1a}} (V_{GS1a} - V_{tn})^2 (\dots)}{K_n' \frac{W_{1b}}{2L_{1b}} (V_{GS1b} - V_{tn})^2 (\dots)} \rightarrow \text{ignore}$$

$$= \frac{W_{1a}}{W_{1b}} = \frac{10.1}{9.9} \qquad \frac{1}{2} - \frac{1}{8} = \frac{1}{16} = 0.06$$

$$\therefore I_{DS1a} = \frac{10.1}{20} \times \frac{1}{8} = 0.063125 mA$$

$$I_{DS2a} = \frac{9.9}{20} \times \frac{1}{8} = 0.061875 mA$$




$$\Delta i_{out} = (I_{SD3b} - I_{ds1b}) = \frac{1}{16}\{1.01 - 0.99\}$$

$$= \frac{1}{8} \times 10^{-5} A$$

$$\Delta V_{out} = \cancel{V_{out2}}\ V_{OUT-2} - V_{OUT}$$

↳ Out prev. $V_{OUT-2}$

$$= R_{out}\,\Delta i_{out}$$

$$= 400k\Omega \times \frac{1}{8} \times 10^{-5} A$$

$$= 0.5V \quad \text{(goes up)}$$

↳ $M_{3b}$ in triode

[$R_{out}$ not exactly 400kΩ]

How to remove discrepancy? $I_{ds1a} > I_{ds1b}$

$\Rightarrow V_{G1a} < V_{G1b}$

$V_{G2a} = (1 - \Delta)V \quad V_{G2b} = (1 + \Delta)V$

so that $V_{OUT2} = V_{OUT2} = 1.8 - 0.55 = 1.25V$

$V_{in-d} = 2\Delta \Rightarrow V_{out} = (2\Delta)\left(-g_{m1}\frac{r_{o1}}{2}\right) = -0.5V$

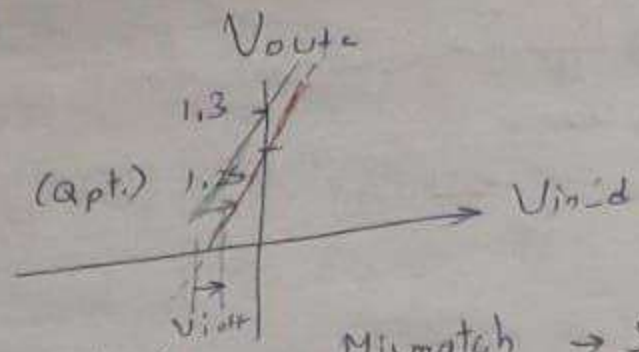
[Should compensate $\Delta V_{out}$]

$$\Rightarrow \Delta = \frac{0.5}{g_{m1} r_{o1}} = \frac{0.5}{200} = 2.5mV$$

$\therefore \Delta = 2.5mV$

0.5 V deviation → Output offset

2.5mV compensation → Input referred offset

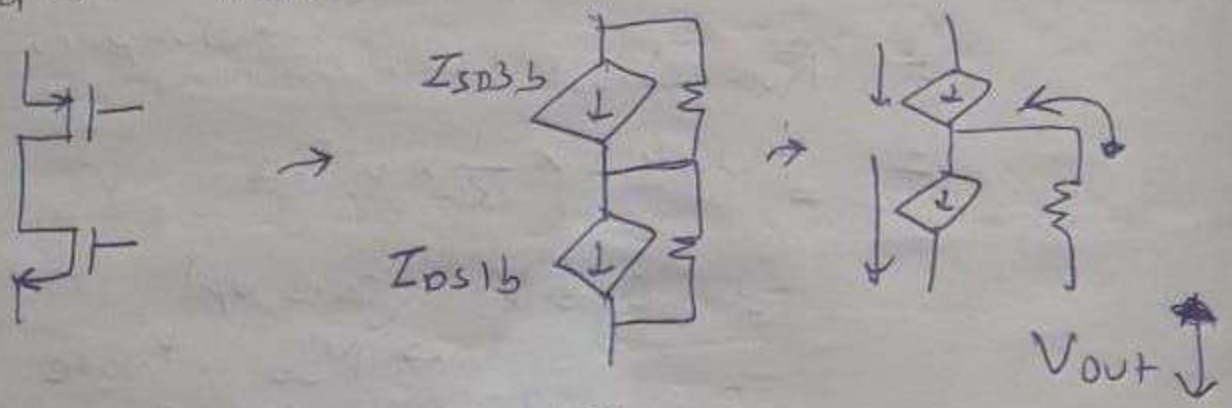



Ideal (Red)

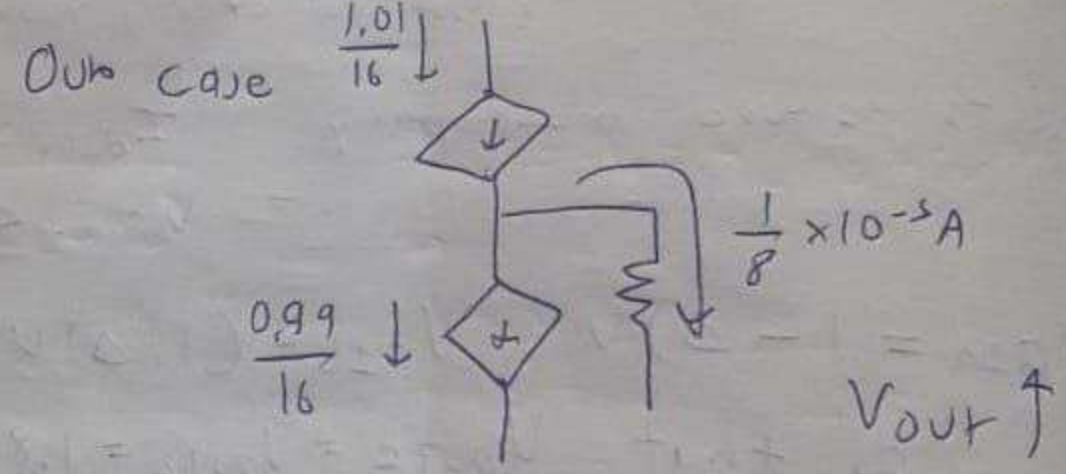
Mismatch (Green) → Shifted up by o/p offset (0.5V)

We want to shift green line to red line. [Shift right by input offset).

Mismatch leads to flow of current in Rout




Our case

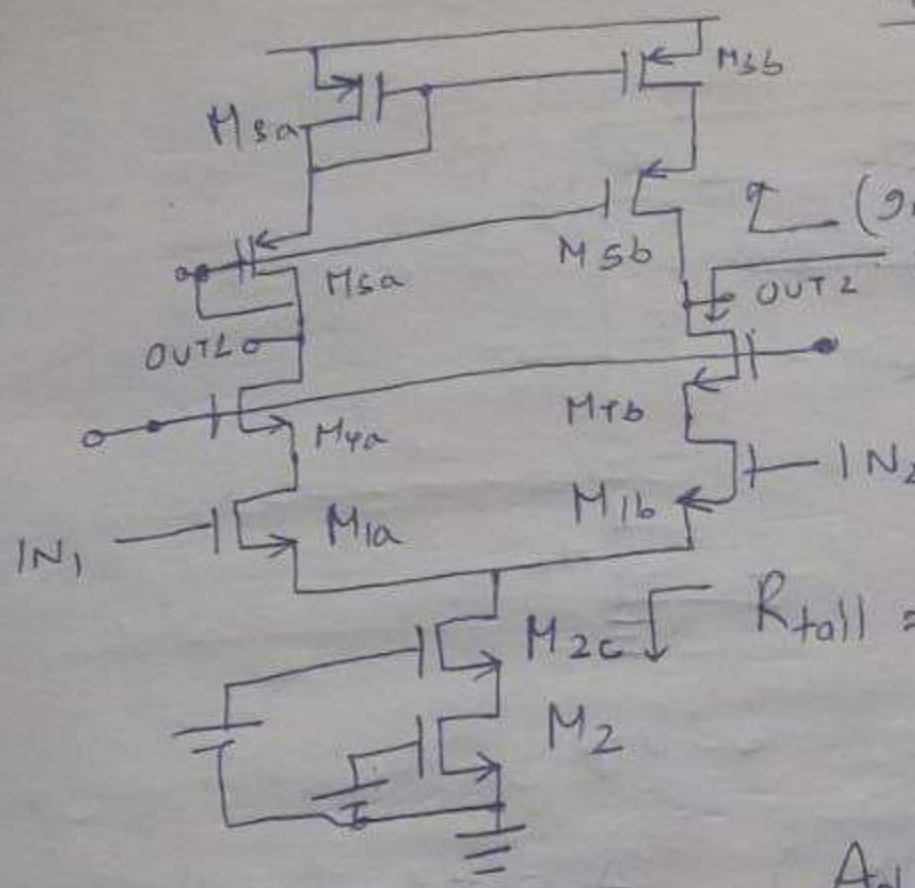



Any signal with $|V_{in-d}| < |V_{in\_offset}|$, signal cannot be amplified with integrity.
Input-referred offset limits circuit capability.

For our diff to single ended amp.

$$A_C = -\frac{1}{g_{m3a}(2r_{o2})}$$

# Telescopic Cascode Amp.




1a, 1b } → More crucial match
3a, 3b }

$g_{m5}r_{o5b})r_{o5b}$ Very high

5, 4 → Not so crucial match

$R_{tail} \approx r_{o2}(g_{m2c}r_{o2c})$

$$A_c \approx -\frac{1}{g_{m3a}(2r_{o2})} \times g_{m2c}r_{o2c}$$

$$A_d = g_{m1}(r_{o3b} \| r_{o1b}) \times g_{m4b}r_{o4b}$$

$$\approx g_{m1}r_{o3b} \quad \text{(Not much improved)} \times (g_{m5}r_{o5b})$$

$$\therefore A_d \approx -g_{m1}(g_{m5}r_{o5b}r_{o3b} \| g_{m4b}r_{o4b}r_{o1b})$$

$$= -g_{m1}\frac{(g_m r_o^2)}{2} \quad \text{[Very high gain]}$$

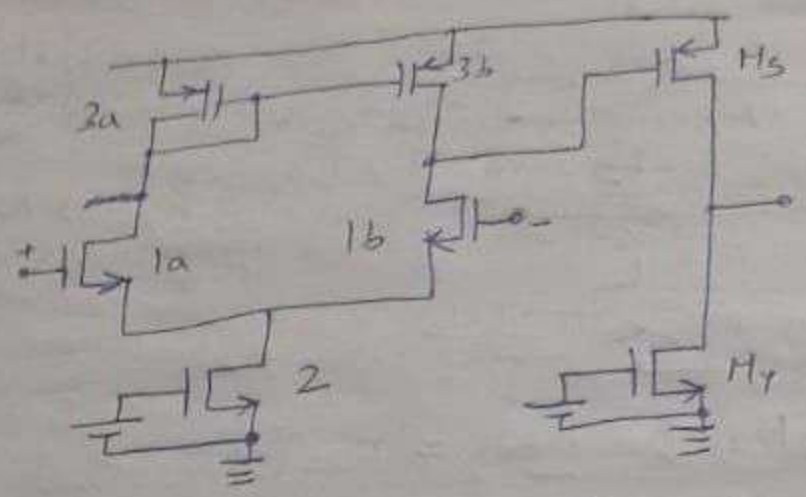
Disadvantage → Voltage swing is low (really low)

[Cannot be used for limited power supply].

But used in small channel technology because $L \downarrow \rightarrow \lambda \uparrow \rightarrow r_o \downarrow \rightarrow A \downarrow$

⇒ Cascode helps in keeping $A \uparrow$.

# 2-stage Amp.




Diff-single CS amp.

$$A_d = -g_{m1}(r_{o3b} \| r_{o1b}) \qquad A_v = -g_{m5}(r_{o5} \| r_{o4})$$

$$\therefore A_{diff} = A_v = A_d A_v = g_{m1} g_{m5} (r_{o3b} \| r_{o1b})(r_{o5} \| r_{o4})$$

$$\approx \frac{(g_m r_o)^2}{4}$$

$$A_{c1} = -\frac{1}{g_{m3a}(2r_{o2})} \qquad A_{c2} = A_v = -g_{m5}(r_{o5} \| r_{o4})$$

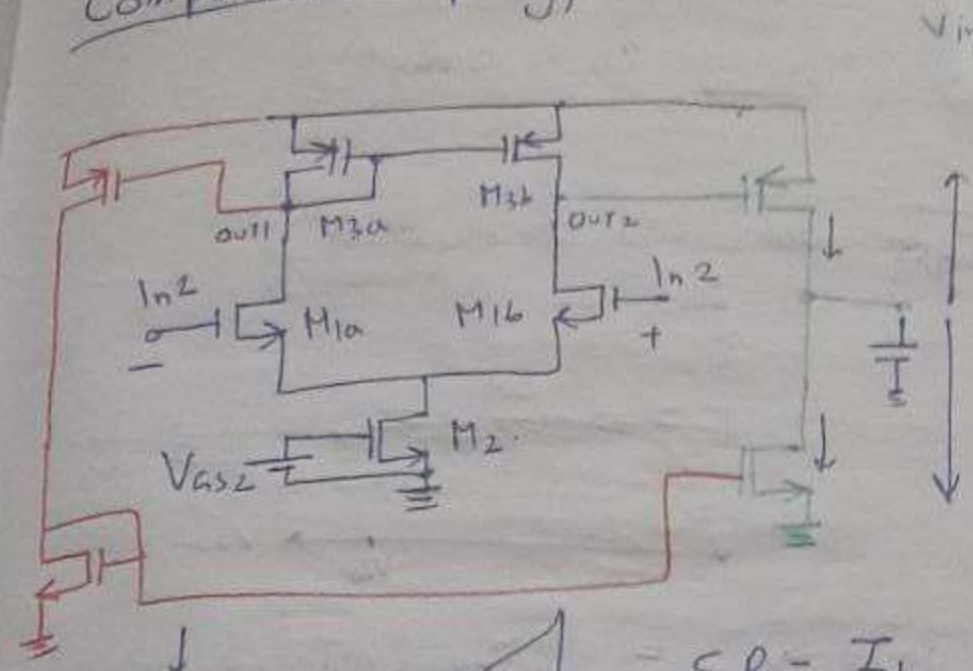
↳ Const distinguish common mode from diff.

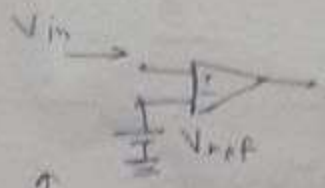
$$A_{cm} = \frac{g_{m5}(r_o)}{g_{m3a}\, 2\times 2 (r_o)} \sim \frac{1}{4}$$

It can work for lower voltage supply and has better swing at output

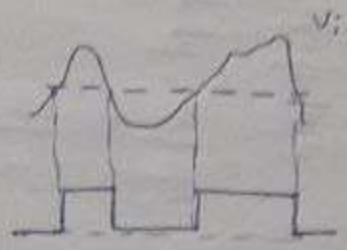
We can use cascode stage in 2nd stage.
We can also use telescopic stage in 1st stage
[Based on reqmt.]

# Comparator Topology




Digital




This connection dynamically changes Slew Rate [Load current is made max.]

$S.R = \frac{I_L}{C_L}$

Static bias $I_L = |I_5 - I_4|$

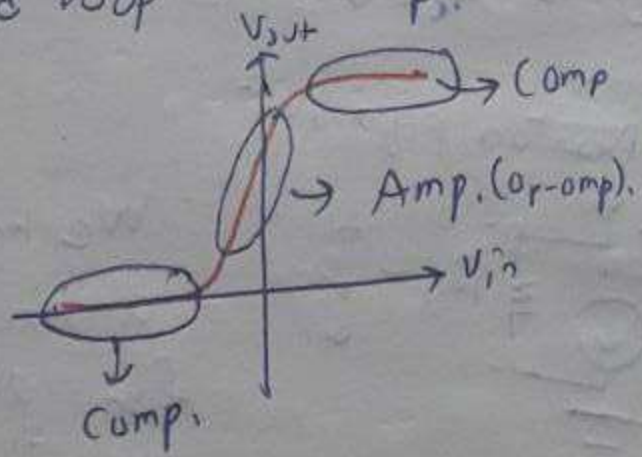
This method $M_5(I) \uparrow \Rightarrow M_4(I) \downarrow$

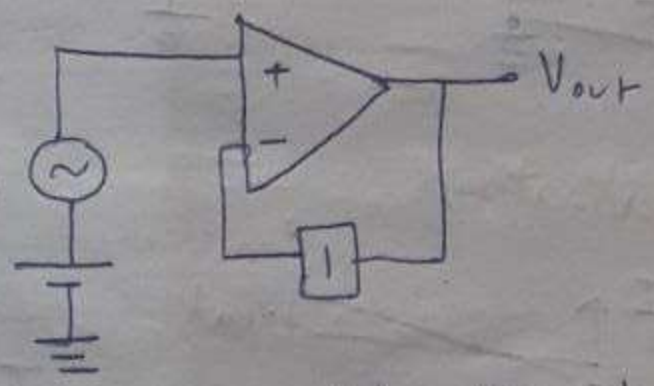
$\Rightarrow I_L \uparrow \Rightarrow S.R \uparrow$

After slewrate improvement $t_{lh}, t_{hl}$ goes down

Open loop → Comparator

Closed loop → Amplifier



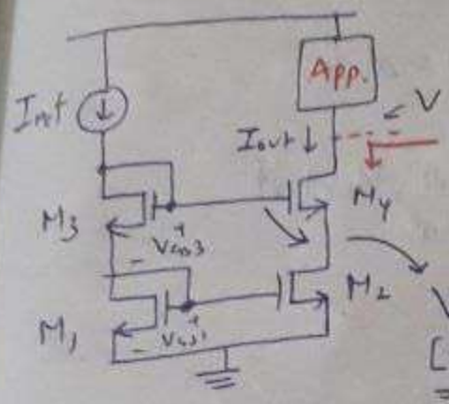




Stability - Very Imp. issue only for amp. (feedback n/w).

Comparator → Cannot be used Via amplifier [OP-AMP should not be used as comp. because f/b network reduces speed of operation].

# Improvement of Current Mirror

## Cascode Current Mirror



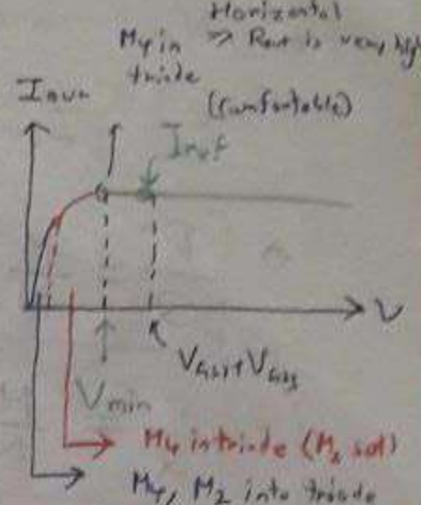

$R_{out} = r_{o2} + r_{o4} + g_{m4} r_{o4} r_{o2}$

$\approx r_{o2}(g_{m4} r_{o4})$

$V_{GS1} + V_{GS3} - V_{GS4}$

$[V_{GS3} = V_{GS4}]$

$\Rightarrow V_{GS2} = V_{GS1}$




$V_{min} = V_{GS1} + V_{GS3} - V_{TH4}$

Output imp. goes up (Advantage)

2 transistors ($M_2$, $M_4$) → $V_{min}$ ↑ (Cost)

$V_{min} = V_{G4} - V_{Th}$

$= V_{GS3} + V_{GS1} - V_{TH4}$ or $V_{dsat4} + V_{GS1}$ [Assuming $V_{GS3} = V_{GS4}$]

At first $M_4$ drops into triode [$\because V_G$

However theoretically through some other implementation, we can go for:-

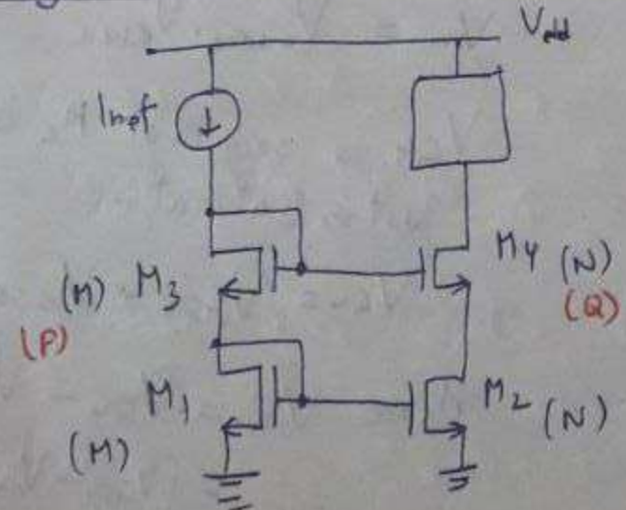
$V_{min} = V_{Dsat2} + V_{Dsat4}$

$= V_{GS1} - V_{Th1} + V_{GS3} - V_{Th3}$

[Scope of improvement] by a $V_{Th}$

Here all devices are of same size. (for this analysis)

## Sizing of Cascode Current Mirror




$\frac{I_{DS4}}{I_{DS3}} = \frac{I_{DS2}}{I_{DS1}} = \frac{N}{M}$

$I_{out} = \frac{N}{M} I_{ref}$

If $M_3$, $M_4$ is $\left(\frac{P}{Q}\right)$ then?

↳ As long as $M_1$, $M_2$ are in saturation.

$I_{out} = \frac{N}{M} I_{ref}$ becomes

$V_{GS1} = V_{GS2}$ but $V_{GS3}$ and $V_{GS4}$ may not be same and can be self adjusting, diff ratio (Q/P).

$V_{DS1}$, $V_{DS2}$ are different.

Hence $I_{out} = \frac{N}{M} I_{ref} [1 + \lambda(V_{DS2} - V_{DS1})]$

* $\frac{P}{Q} = \frac{M}{N} \Rightarrow V_{DS2} = V_{DS1}$ → Full match

$\frac{P}{Q} \neq \frac{M}{N} \Rightarrow V_{DS2} \neq V_{DS1}$ → Small effect of mismatch

$V_{GS3} = V_{GS4}$

and $V_{GS3} + V_{GS1} - V_{GS4} = V_{DS2}$

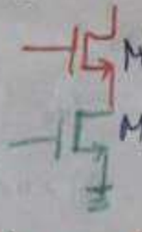
$\Rightarrow V_{GS1} = V_{DS1} = V_{DS2}$

Hence $M_1$ and $M_2$ sizing, matching is crucial compared to $M_3$ and $M_4$ (may be relaxed).

$R_{out} = r_{o2}(g_{m4} r_{o4})$ [Lost attention. Watch video]

Individual element of $M_2$ and $M_4$ need not be same.

We go for $L_4 = L_{min}$, to reduce lower limit of $V_{min}$

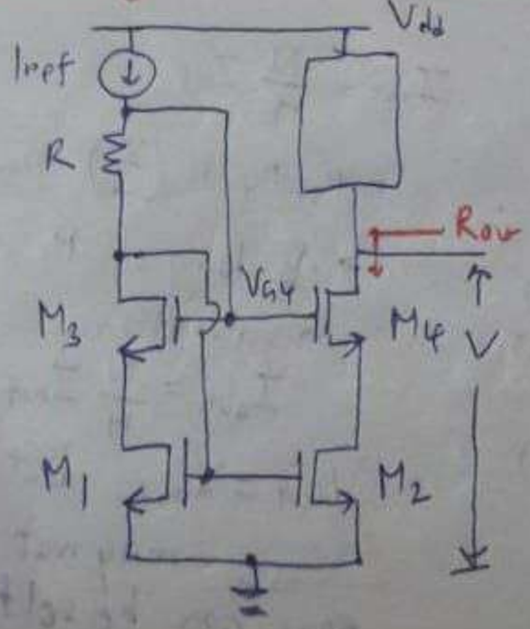



$L_2 > L_4 = L_{min}$ ; $W_3 = W_4$

$V_{GS3} - V_{Th}$ reduces

$\frac{W_4}{L_4} > \frac{W_2}{L_2}$ → same current (less $V_{GS} - V_{Th}$)

## Wide swing Cascode Current Mirror




$V_{min} = V_{dsat2} + V_{dsat4}$

$V_{G4}$ is such that $M_2$ is just in saturation.

$V_{G4} = V_{GS4} + V_{dsat2}$

Hence $V_{min} = V_{G4} - V_{th}$

$= (V_{GS4} - V_{th}) + V_{dsat2}$

$= V_{dsat4} + V_{dsat2}$

We tune $R_4$ to set $V_{G4}$. [$R_{out} = r_{o2} g_{m4} r_{o4} + r_{o2} + r_{o4}$]

$$V_{G4} = V_{GS1} + I_{ref} R$$

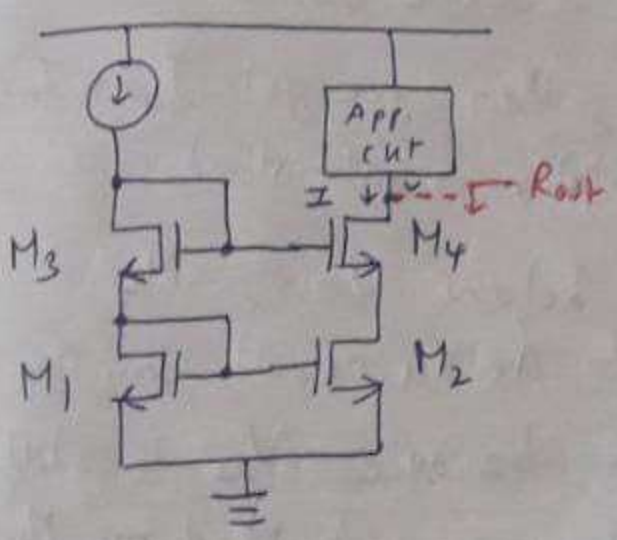
↓ Flexibility

[Earlier $V_{G4} = V_{GS1} + V_{GS3}$] ↓ No flexibility

This circuit lowers $V_{min}$ → Hence wide swing.

## Re-iteration from Improvement of Current Mirror

### Cascode Current Mirror

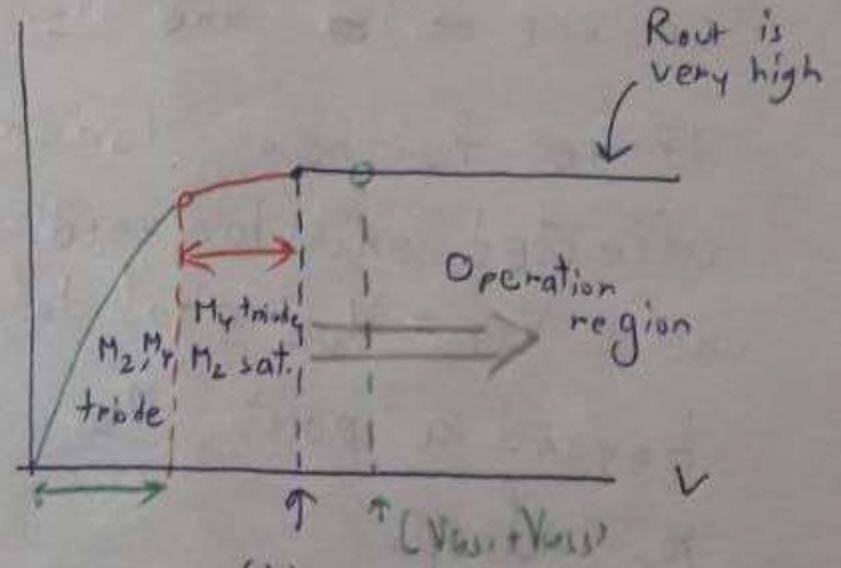



For the time being let us ignore $M_3$ and we supply a dc voltage at gate of $M_4$.

We then look into drain of $M_4$ and see its impedance

$$R_{out} = r_{o2} + r_{o4} + r_{o2}(g_{m4} r_{o4})$$
$$\approx r_{o2}(g_{m4} r_{o4})$$

Now we plot I vs V




As $R_{out}$ is now quite large, I is almost "independent" of V.

[Both $M_4$ and $M_2$ in saturation]

However it is important that we have to keep both $M_4$ and $M_2$ in saturation.

$$\therefore V_{min} = V_{G4} - V_{Tn4} \quad [\text{For } M_2, M_4 \text{ in saturation}]$$
$$= V_{GS1} + V_{GS3} - V_{Tn4}$$

If we consider that $V_{D4}$ and $V_{D3}$ are equal, this ensures that $V_{GS3}$ and $V_{GS4}$ are equal. Likewise $V_{GS2}$ and $V_{GS1}$ are equal.
This is done considering (W/L) of all transistor are equal.

$$V_{D2} = V_{GS1} + V_{GS3} - V_{GS4}$$

Now we say that 3,4 are identical.

$$\Rightarrow V_{GS3} = V_{GS4}$$

$$\therefore V_{D2} = V_{GS1} = V_{GS1} \rightarrow \text{Same current}$$

Hence if $V_{out} = V_{GS1} + V_{GS3}$, then we get $I_{out} = I_{ref}$.
(both $M_4$, $M_2$ are comfortably in saturation)

However if I reduce V below $V_{min}$, $M_4$ almost enters into triode. As a result $g_{m4} r_{O4}$ drops but $r_{O2}$ is still high because $V_{O2}$ is still not very low (as per Razavi - shielded by $M_4$ cascode →) and $M_2$ remains in saturation

If we further lower V, then $V_{O2}$ will get affected and lowered ($V_{GS4}$ cannot be less than 0; hence $V_{S4} = V_{O2}$ has to follow $V_{D4} = V$) and beyond a point $M_2$ gets into triode. Also $r_{O2}$ drops.

Hence output impedance ↑ (Advantage)

But Voltage limit ↑ (Cost)

$V_{min} = V_{GS1} + V_{GS3} - V_{th4}$ is a hard limit

Significant↓ compared to $V_{dd}$ in submicron

$V_{gs1} + V_{gs3} - V_{th4} = V_{gs1} + V_{gs4} - V_{th4}$ (We said earlier $V_{gs3} = V_{gs4}$ some dis.)
$= V_{gs1} + V_{dsat4}$

However we don't need $V_{gs1}$ as a bare minimum to keep $M_2$ in saturation. We require $V_{dsat2}$.

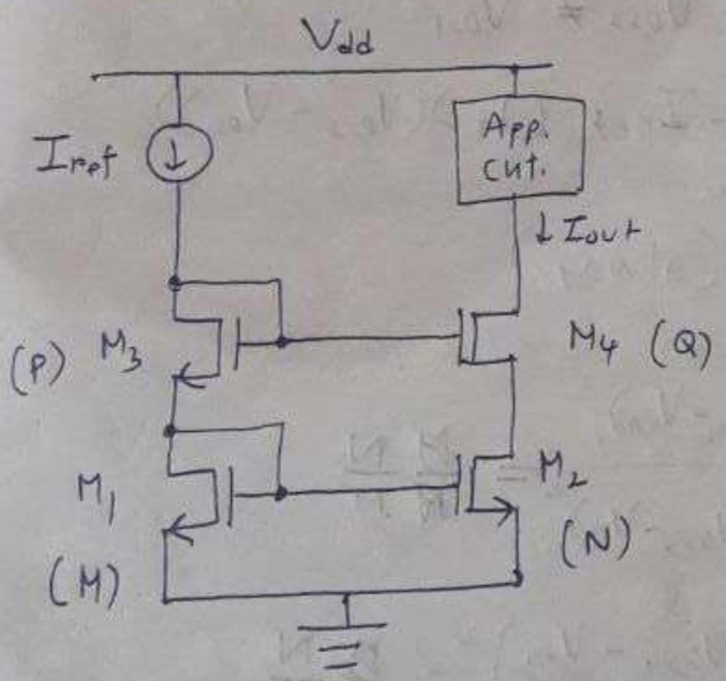
Theoretical limit → $V_{min_{th}} = V_{dsat2} + V_{dsat4}$ (can be obtained in different implementation if $V_{gs4}$ can be modified)

$[V_{gs1} = V_{gs2}]$
$= (V_{gs1} - V_{th_2}) + (V_{gs4} - V_{th4})$

comparing with original $V_{min}$, there is a scope of improvement by $V_{th2}$.

$I_{out} = I_{ref} \times \left(\frac{N}{M}\right)$ → Modifying number of transistors

## Sizing of Cascode Current Mirror




If $M_3 : M_4 \Rightarrow P : Q$ in place of $M:N$; What will be $I_{ref}$ - $I_{out}$ relation?

Ans: $I_{out} = \frac{N}{M} I_{ref}$

$V_{gs1} = V_{gs2}$
$\Rightarrow I_{out} = \frac{N}{M} I_{ref}$

[Fixed and dominating as long as $M_1, M_2$ in saturation]

Is it independent of Q/P?
↳ Yes; Because $V_{gs4}$ is self adjusting to support $I_{out}$ through it.

$V_{gs1}, V_{gs3}$ → Self generated by diode equation as $I_{ref}$ is fixed

$\Rightarrow \frac{I_{DS4}}{I_{DS3}} = \frac{I_{DS2}}{I_{DS1}}$

[Only thing is that $V_{gs3} \neq V_{gs4}$ because $\frac{P}{Q} \neq \frac{M}{N}$]

As $V_{GS3} \neq V_{GS4}$ $\left[\text{For } \frac{P}{Q} \neq \frac{M}{N}\right]$ — (α)

$\Rightarrow V_{G3} - V_{S3} \neq V_{G4} - V_{S4}$

But $V_{G3} = V_{G4}$

$\Rightarrow V_{S3} \neq V_{S4}$

$\Rightarrow V_{DS1} \neq V_{DS2}$

$\therefore I_{out} = \frac{N}{M} I_{ref} \left(1 + \lambda(V_{DS2} - V_{DS1})\right)$

Hence $\frac{P}{Q} = \frac{M}{N} \Rightarrow V_{GS3} = V_{GS4}$ — (β)

$\Rightarrow V_{DS2} = V_{DS1}$

$\therefore I_{out} = \frac{N}{M} I_{ref}$

And for $\frac{P}{Q} \neq \frac{M}{N} \Rightarrow V_{GS3} \neq V_{GS4}$

$\Rightarrow V_{DS2} \neq V_{DS1}$

$\therefore I_{out} = \frac{N}{M} I_{ref} \left(1 + \lambda(V_{DS2} - V_{DS1})\right)$

$\frac{I_{DS2}}{I_{DS1}} = \frac{I_{DS4}}{I_{DS3}} = \frac{N}{M}$ (always)

$\Rightarrow \frac{\frac{K_n'}{2}\left(\frac{W}{L}\right)_4 (V_{GS4} - V_{tn})^2}{\frac{K_p'}{2}\left(\frac{W}{L}\right)_3 (V_{GS3} - V_{tn})^2} = \frac{N}{M}$

$\Rightarrow \frac{Q}{P}\left[\frac{V_{GS4} - V_{tn}}{V_{GS3} - V_{tn}}\right]^2 = \frac{N}{M}$

$\Rightarrow \boxed{\left[\frac{V_{GS4} - V_{tn}}{V_{GS3} - V_{tn}}\right]^2 = \frac{N}{M} \times \frac{P}{Q}}$

This result helps us conclude α and β.

Thus | Sizing of $M_1$ and $M_2$ is crucial for $I_{out}/I_{ref}$ ratio. whereas $M_3$ and $M_4$ sizing is relaxed

As long as everybody is in saturation, $R_{out} \approx r_{o2}(g_{m4} r_{o4})$ [Quite high]

We want to keep $L_{\bullet}$ ~~Greater~~ $L > L_{min}$.

Reason: Due to process variation we have $L + \Delta L$, $\Delta L$ is fixed by technology; hence to reduce % variation we take a higher $L$. For good matching of 1, 2 this is essential. [All elements must be matched individually].

$\therefore L_1, L_2 \rightarrow$ non-minimum.

Based on earlier discussion; matching of $M_3$ and $M_4$ is not essential/crucial; hence mismatch is not an issue. $\therefore$

$\therefore L_3, L_4 = L_{min}$

Moreover matching of (1 and 2) with (3 and 4) is not essential. → (Individual element matching not essential)

We take $W_4 = W_2$

↓

For good layout.

$M_4 \neq M_2$ $M_3 \neq M_1$

$L_3$ $[L_2 > L_4 = L_{min}]$

We go for $L_4 = L_{min}$ for one very imp. reason

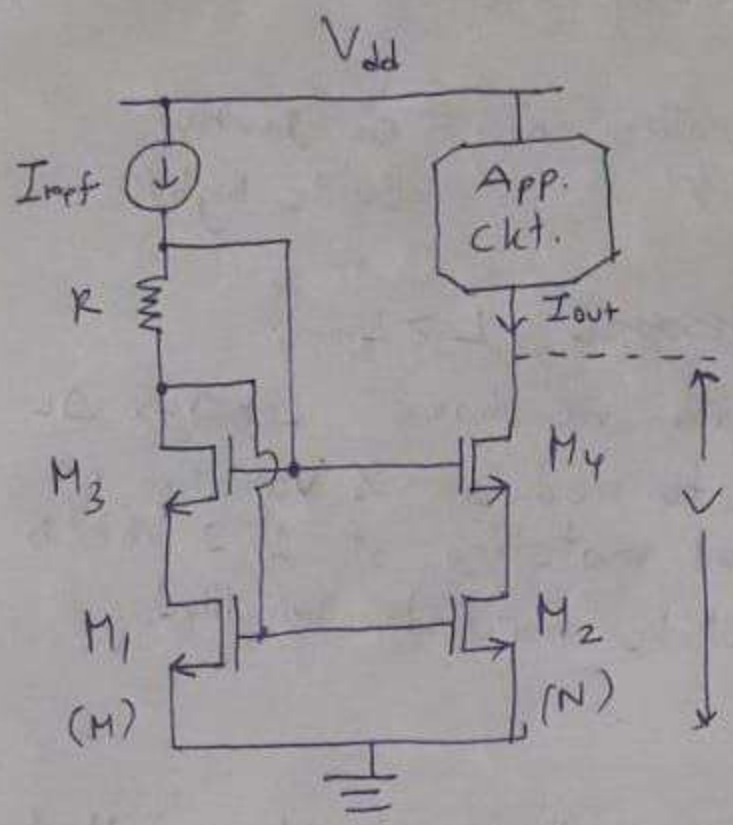
$\therefore \left(\frac{W_3}{L_3}\right) \frac{W_4}{L_4} \uparrow \Rightarrow$ For same $I_{os}$ $[W_4 = W_2]$

$V_{gs4} \downarrow$ ($V_{gs3} \downarrow$)

$\Rightarrow$ This reduces the $V_{dsat4}, V_{dsat3}$ (helpful for $v_s$ - lowering the $V_{min}$ indirectly)

$V_{dsat4} < V_{dsat2}$

# Wide Swing Cascode Current Mirror




Prev design:

$V_{min} = V_{GS1} + V_{GS3} - V_{TH}$

$= V_{GS1} + V_{dsat4}$

If we keep flexibility on $V_{G4}$.

$V_{min} = V_{dsat2} + V_{dsat4}$

(Theoretical lowest)

$V_{G4} = V_{GS4}$ (Q6) $+ V_{dsat2}$ ($M_2$ in sat)

$V_{G4} - V_{th} = V_{dsat2} + V_{dsat4}$ ($V_{min}$)

By making an arrangement, we introduce flexibility in $V_{G4}$. [Tuning of R]

$\therefore V_{D4}|_{min} = V_{G4} - V_{th4}$

$= V_{GS4} - V_{th4} + V_{dsat2}$

$= V_{dsat4} + V_{dsat2}$

$R_{out} = (g_{m4} r_{o4}) r_{o2} + r_{o2} + r_{o4}$ [Same as earlier]

Voltage limit = $V_{dsat2} + V_{dsat4}$

* $V_{G4} = V_{G3} + I_{ref} R$

$= V_{GS1} + I_{ref} R$ [Earlier we had $V_{GS1} + \underbrace{V_{GS3}}_{\text{fixed}}$]

[$V_{GS1} + I_{ref} R = V_{dsat2} + V_{GS4}$]

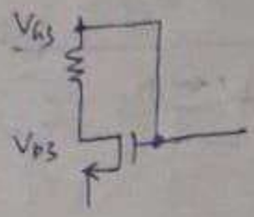
$I_{out} = \frac{N}{M} I_{ref} (1 + \lambda (V_{DS2} - V_{DS1}))$

## Sizing of Wide swing cascode current mirror

$$V_{GS3} - V_{D3} \leq V_{th3}$$

$$\Rightarrow \boxed{I_{ref} R \leq V_{th3}}$$

↳ $M_3$ in saturation

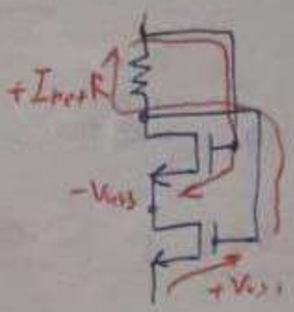



$M_1$ in saturation

$$V_{D1} \geq V_{G1} - V_{th1}$$

$$\Rightarrow V_{GS1} + I_{ref} R - V_{GS3} \geq V_{GS1} - V_{th1}$$

$$\Rightarrow \boxed{I_{ref} R \geq V_{GS3} - V_{th3}}$$




We choose $I_{ref} R$ as mid point of $V_{th3}$ and $(V_{GS3} - V_{th3})$.

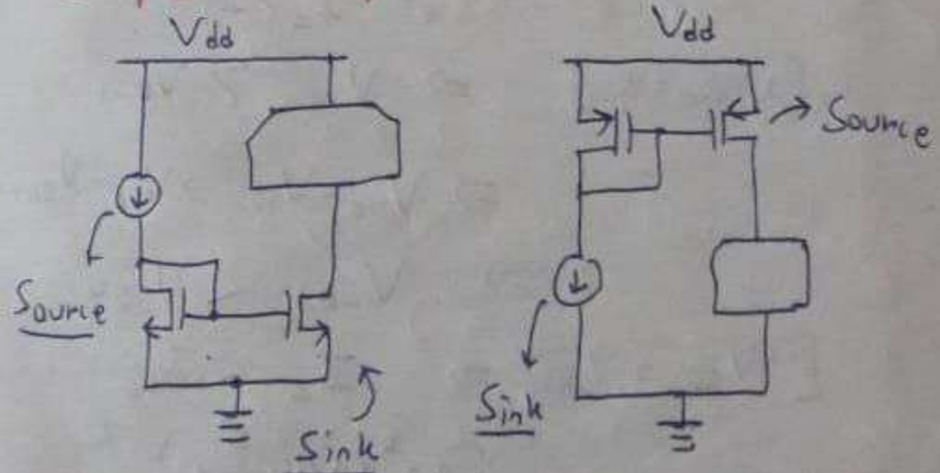
Again $M_1, M_2 \rightarrow L$ be high

$M_3, M_4 \rightarrow L = L_{min}$ so that $(V_{GS} - V_{th}) \downarrow$ and $W_4 = W_2$.

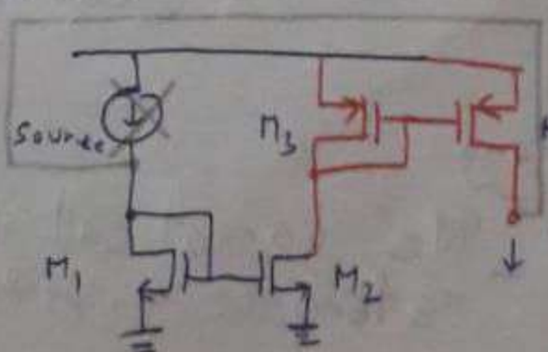
## Week-7 (12/10/20)

## Current Reference Circuit

Simple Attempt:

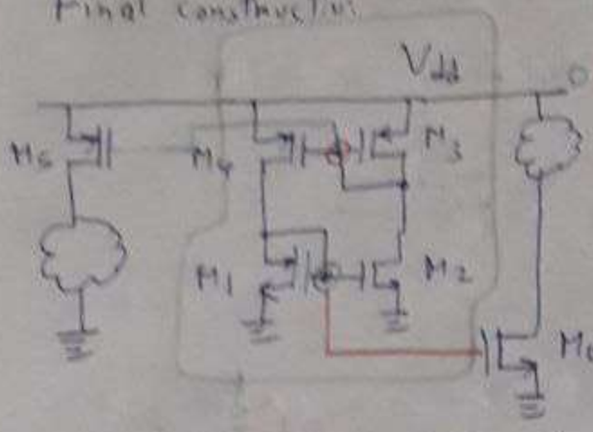



Source - Source




→ Can we use it directly (– flow)

Final construction



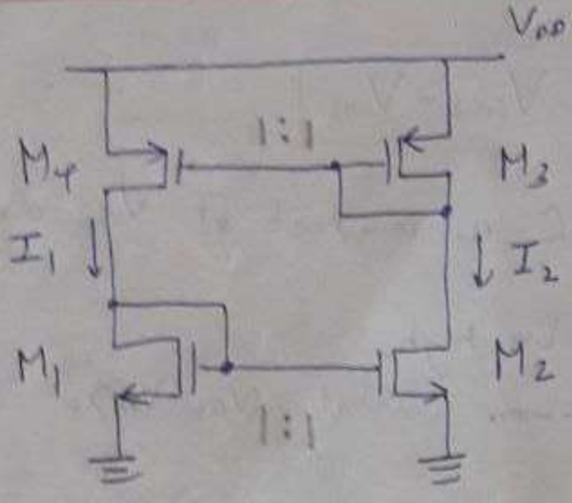

o o → Can be utilised for extension [to get another current source]

$M_3, M_5$ → Current mirror

$M_1, M_6$ → Current mirror pair

Who defines $I_{ref}$?

## Issue in Simple Construction




$I_1 = I_{DS1} = I_{SD4}$

$I_2 = I_{DS2} = I_{SD3}$

Hence

$I_1 = I_2$ $[\because V_{GS1} = V_{GS2}]$

$\Rightarrow V_{DS2} = V_{DS1}$

$\hookrightarrow V_{GS1} = V_{DS2}$

$\hookrightarrow V_{SG3} = V_{SD3}$

$\Rightarrow V_{GS1} + V_{SG3} = V_{dd}$

$I_1$ & $I_2$ are strong function of $V_{dd}$. [We cannot call it a good reference → dependency on $V_{dd}$]

$\lambda \approx 0$

$\hookrightarrow I_2 = I_1$

(No issues)

What is its value?

[We cannot find any answer]

$\lambda \neq 0$

$\hookrightarrow I_1 = I_2$

Proof:

Let $I_2 > I_1$

$\Rightarrow V_{DS2} > V_{DS1}$

$\Rightarrow V_{DD} - V_{SD3} > V_{DD} - V_{SD4}$

$\Rightarrow V_{SD3} < V_{SD4}$

$[\because V_{SG4} = V_{SG3}] \Rightarrow I_2 < I_1$

(Contradiction)

$$I_1 = \frac{K_n'}{2}\left(\frac{W}{L}\right)(V_{GS1} - V_{th})^2(\ldots)$$

$$I_2 = \frac{K_p'}{2}\left(\frac{W}{L}\right)(V_{SG3} - V_{th})^2(\ldots)$$

$$V_{GS1} + V_{SG3} = V_{dd}$$

$$I_1 = I_2$$

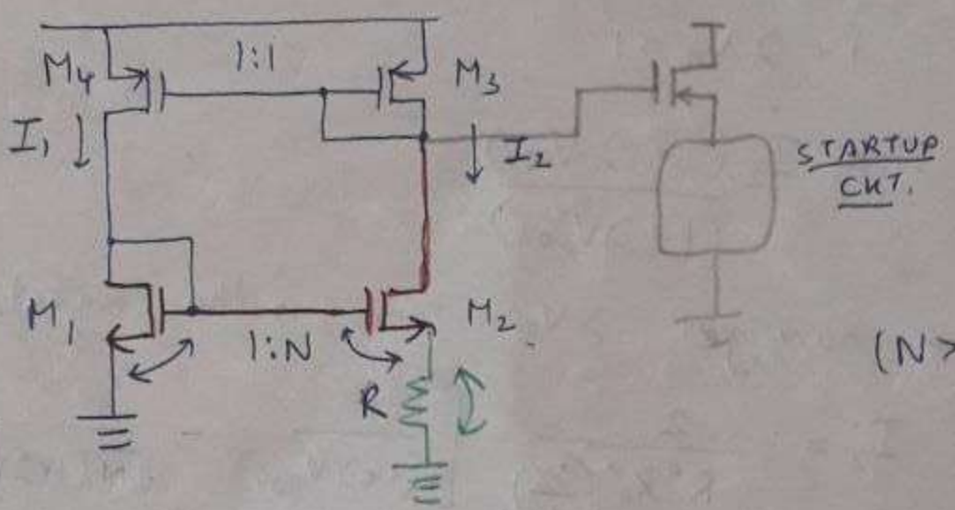
4 eq; 4 variable

→ $I_1$, $I_2$ fixed by $V_{dd}$ variation and $V_{th}$ variation (due to process $V_{dd} \to V_{th}$ var.) make this unsuitable.

If $V_{dd}$ was ideal, we could have used this circuit well.

Construction of Current Reference -

## Basic Structure and Analysis:




(N>1)

Let us first ignore $\lambda$:

$$V_{GS1} = V_{GS2} + IR_{drop}$$

- $I_1 = I_2$
- $V_{GS1} = V_{GS2} + I_2 R \quad \to [V_{GS2} < V_{GS1} \Rightarrow N > 1 \text{ !balance}]$

$$\Rightarrow \sqrt{\frac{2I_1}{K_n'\left(\frac{W_1}{L_1}\right)}} + V_{th_1} = \sqrt{\frac{2I_2}{K_n'\left(\frac{W_2}{L_2}\right)}} + V_{th_2} + I_2 R$$

$$V_{th1} = V_{th2}$$

$$\Rightarrow \left(\sqrt{\frac{2L_1}{K_n'W_1}} - \sqrt{\frac{2L_2}{K_n'W_2}}\right)\sqrt{I_2} = I_2 R \quad \text{— } (\alpha)$$

$$(W_2 = NW_1);\ (L_1 = L_2)$$

$$\Rightarrow \sqrt{I_2} = \frac{1}{R}\sqrt{\frac{2L_1}{K_n' W_1}}\left[1 - \frac{1}{\sqrt{N}}\right]$$

$$\therefore \boxed{I_2 = \frac{2}{R^2 K_n' \left(\frac{W}{L}\right)_1}\left[1 - \frac{1}{\sqrt{N}}\right]^2} \rightarrow \text{No dependence on } V_{DD}$$

[Only for $1+\lambda V_{DS} \approx 1$]

If $N=1$ and $R \neq 0 \rightarrow I_2 = 0$ (Forced to be in cutoff)

$N<1 \rightarrow$ also means $M_2$ in cutoff [$I_2$ ignored]

$N = 4, 8, \ldots$ [Integer for good match

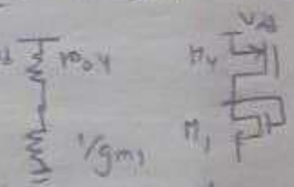
** If $1 + \lambda V_{DS} = 1$

$$\Rightarrow I_1 = I_2 \frac{(1+\lambda V_{SD4})}{(1+\lambda V_{SD3})}$$

We now get $\lambda V_{DS}$ terms in the equation.

$$I_2 = \frac{2}{R^2 K_n' \left(\frac{W}{L}\right)_1}\left[\frac{1}{(1+\lambda V_{SD4})} - \frac{1}{\sqrt{N}(1+\lambda V_{SD3})}\right]$$

$V_{GS1}$
$V_{DS1} + V_{SD4} = V_{DD}$




$V_{DD}$ variation ↓
Negligible effect on $V_{GS1}$ ($\because \frac{1}{g_{m1}} \ll r_{o4}$)

→ Cascoding can reduce dependency by a factor of $(g_m r_o)$.

Issue: In equation (α), we have ignored another solution i.e. $\sqrt{I_2} = 0$

→ Thus we have 2 possible values of $I_2$ including 0. And $I_2 = 0$ also mean stable circuit.

This is called <u>startup issue</u>. If $I_2 = 0$ at starting of circuit, it will remain in this state forever

We need another circuit to mitigate this. We sense the current and if $I_2 = 0$, we trigger something called STARTUP ckt.

13/10/20

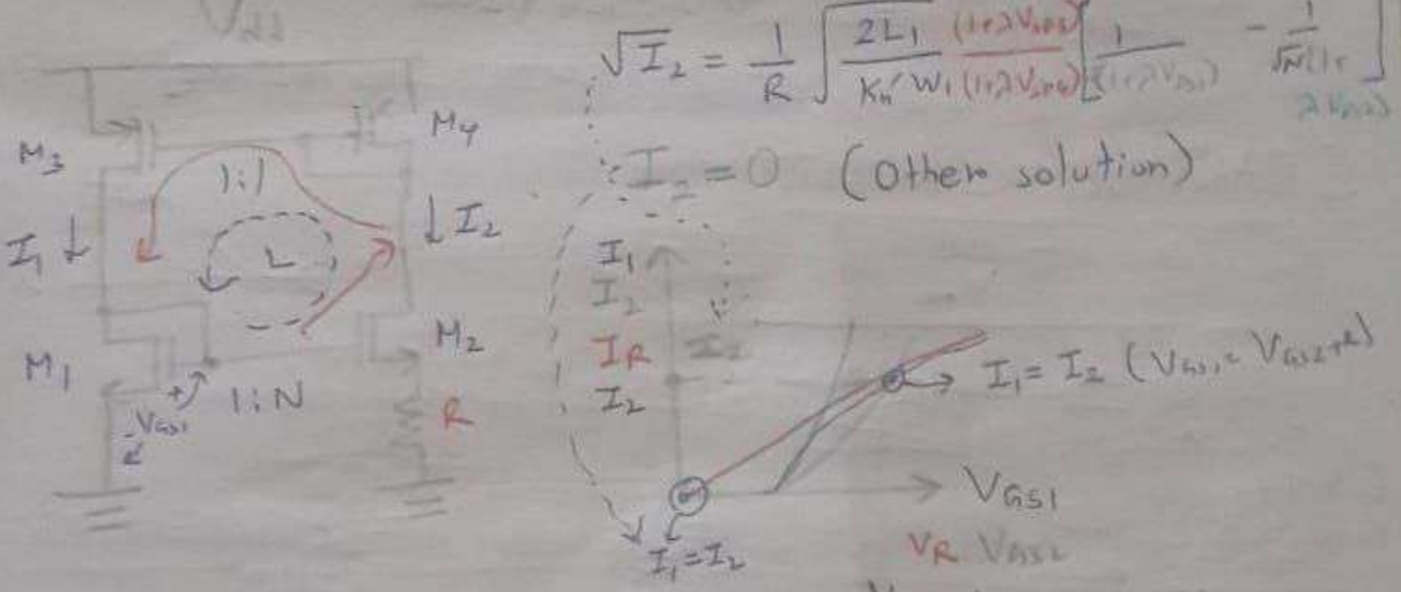
## Current Reference

Basic Structure and Analysis:

$[V_{GS2} + I_2 R = V_{GS1}]$ Root equation

$$\sqrt{I_2} = \frac{1}{R}\sqrt{\frac{2L_1}{K_n' W_1}\cdot\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})}}\left[\frac{1}{\sqrt{(1+\lambda V_{DS1})}} - \frac{1}{\sqrt{N}(1+\lambda \frac{V_{DS2}}{2})}\right]$$

$\therefore I_2 = 0$ (other solution)




Blue line follows green curve and then red. [Dominated by lowest current among $M_2$, R]

Circuit has positive feedback. (L)

↳ Ensure no oscillation.

$\Rightarrow |L| < 1$ $[G_{M2} \to D_{M4} = G_{M4} \to D_{M1} = G_{M2}]$ G → Gate, D → Drain

$[g_{m3} = g_{m4}]$

↳ $-\left(\frac{g_{m2}}{1+g_{m2}R}\cdot\frac{1}{g_{m4}}\right)\cdot\frac{g_{m3}}{g_{m1}}$

$= \frac{g_{m2}}{g_{m1}}\cdot\left(\frac{1}{1+g_{m2}R}\right)$

$= \frac{\sqrt{N}}{1+g_{m2}R}$

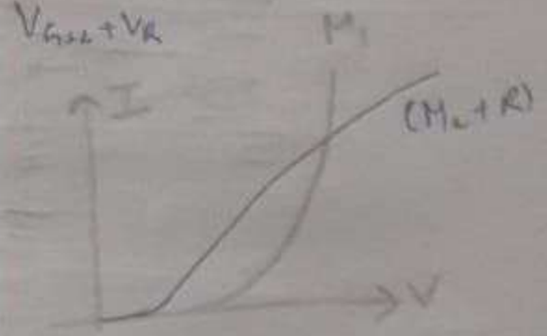
$= \frac{\sqrt{N}}{1+2\sqrt{N}-2} = \frac{\sqrt{N}}{2\sqrt{N}-1} = \frac{1}{2-\frac{1}{\sqrt{N}}}$

$g_{m2}R = \sqrt{2K_n'\left(\frac{W}{L}\right)_2 I_2}\,R$

$= \sqrt{2NK_n'\frac{W_1}{L_1}I_2}\cdot R$

$= 2\sqrt{N}\left(1-\frac{1}{\sqrt{N}}\right)$

$= 2(\sqrt{N}-1)$

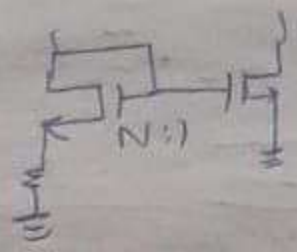


$N=1 \Rightarrow L=1$ (Unstable → oscillation)

$N>1 \Rightarrow |L|<1$ → Stable

$N<1$ → Blue and pencil line never intersect apart from origin ($I=0$)

Suppose we do →

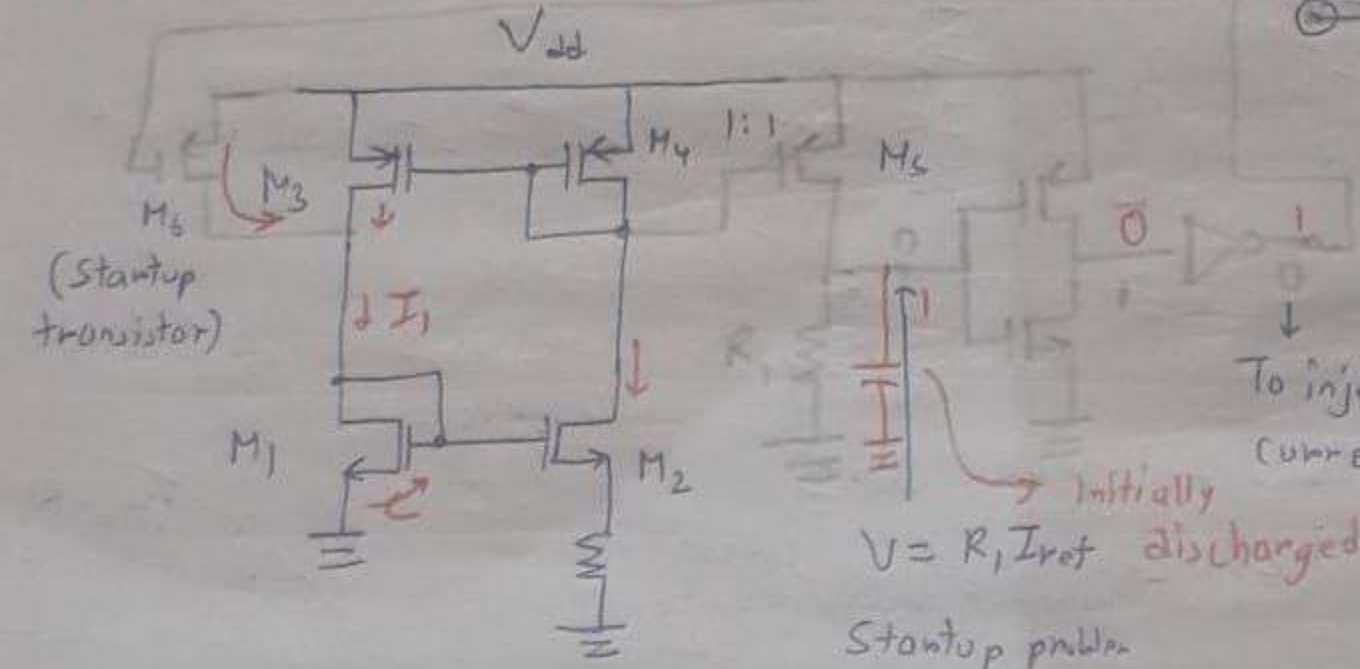



→ Loop gain always $>1$ (for $N>1$)

→ Unstable ($I=0$)

[DONT COMMIT THIS MISTAKE]

## START-UP CIRCUIT




[Ensures that startup ckt doesn't become too fast]

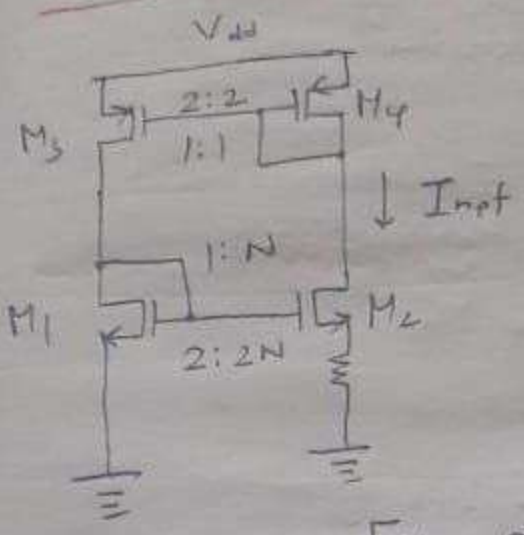
Just afterwon : $I_1 = I_{M3} + I_{M6} > I_2$ and beyond stable

(We chose $I_{ref}$ $V > 0$ ↑ and all values invert and back to stable and startup become Off)

When completely on, $I_{ref}$ $R_1$ should be high enough so that $M_6$ is fully off. [Shouldn't be weakly on.]

This is present in every chip.

# Values of W's, L's and R




$$I_{ref} = \frac{R_1}{R^2} \cdot \frac{2L_1}{K_n' W_1} \left(1 - \frac{1}{\sqrt{N}}\right)^2$$

N = 4 (Good match)

For better match → 2:2N
(Layout) → 2:2

$L_1 = 1\mu$

For given $I_{ref}$; $W_1$, $W_4$ should be such that $V_{GS1}$ is determined/defined to satisfy this

$V_{dd\_min} = \max\{V_{GS1} + V_{SG4} - V_{th0},\ V_{GS1} + V_{SG4} - |V_{thp}|\}$ ← $V_{SG4}$,

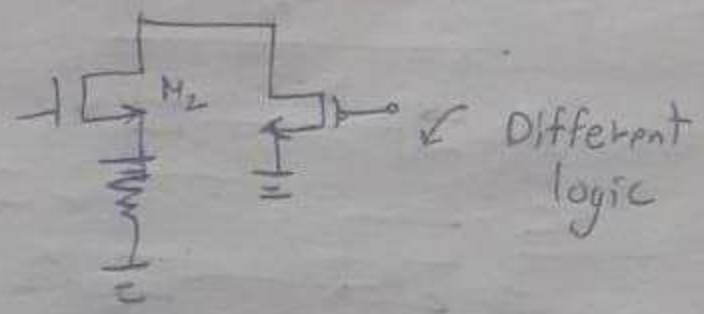
Better understanding:

$$V_{dd} > (V_{GS1} - V_{th1}) + (V_{SG4} - |V_{thp}|)$$

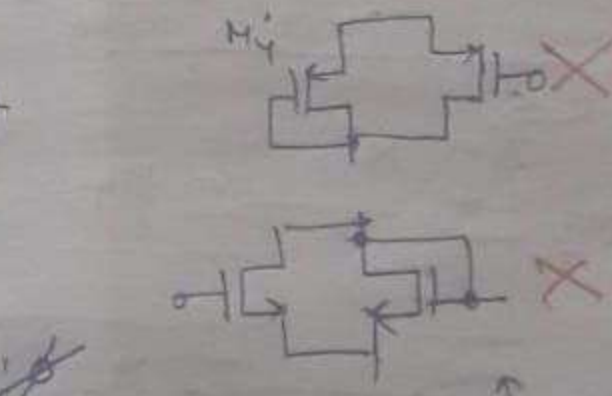
$R_1 I_{ref} > V_{inv}$ [Startup circuit]
↳ [$V_{TH}$ of inverter]
[Proper detection of on]

[Keeps $M_2, M_3$ in saturation]

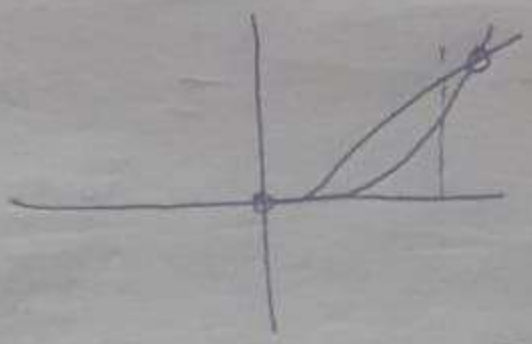
Instead of $M_6$, we can have:

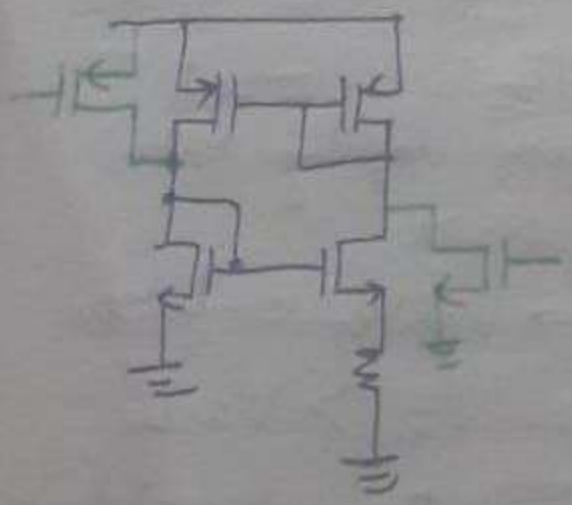



Different logic

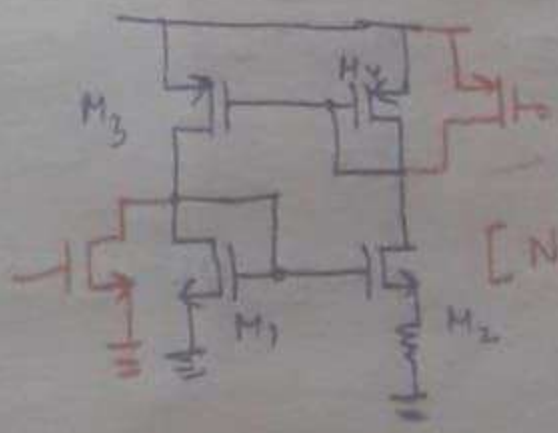



Current injection actually reduces (NMOS i-p.)





Either way this works
correct for current injection




[Never do these]

Not working

If we use one of the wrong config, say NMOS imp.

→ current through $M_1$ reduces [Extra logic NMOS sucks the current]

→ reduced current through $M_1$ is mirrored by $M_2$ and then to $M_3$ via $M_4$.

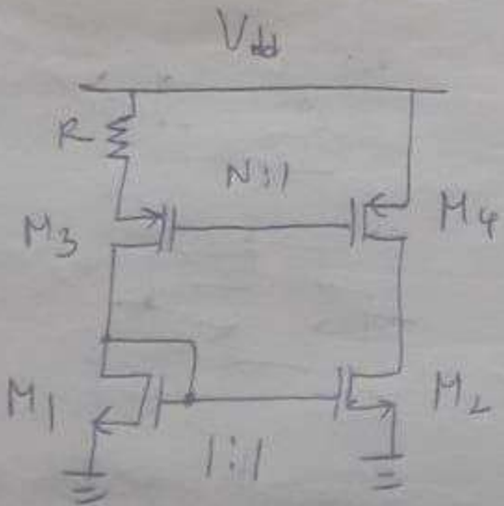
→ $I_{M3} = I_{M1} + I_{extra}$

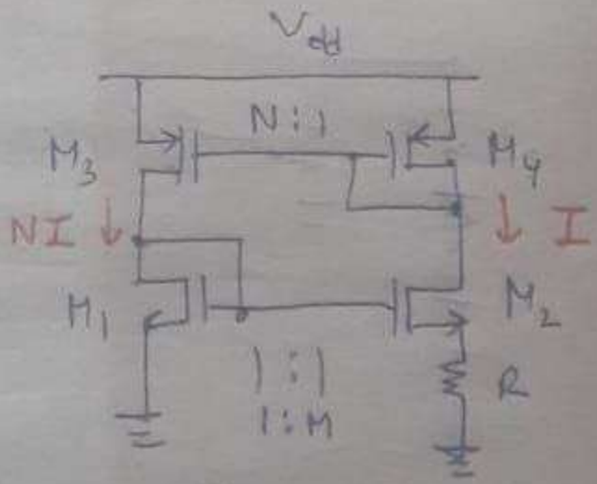
$M_3$ is already reduced and $I_{extra}$ again reduces it decreasing $I_{M1}$ further.

Thus I in system remains 0.

This thing happens.

## VARIANTS AND IMPROVEMENTS OF CURRENT REF:




To keep

$V_{GS1} > V_{GS2}$ (IR>0)

Always ensure

$V_{SG3} < V_{SG4}$

to ensure drop across R

$M_3 : M_4$ is current mirror defining ratio

$M, N > 1$

↳ double reinforces

$V_{GS1} > V_{GS2}$

($W \uparrow \Rightarrow V_{GS} \downarrow$)

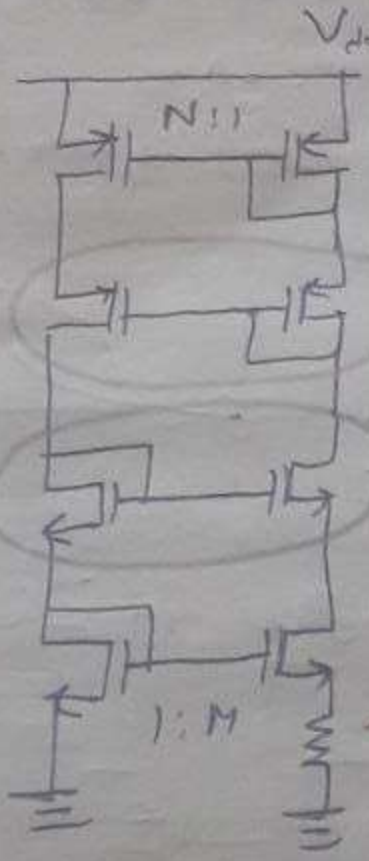
$I_2 = [\ ]\ \frac{(\ )}{(\ )}\left[\frac{1}{(\ )} - \frac{1}{\sqrt{N}(\ )}\right]$

1st order $\lambda V_{DS}$ terms

$\lambda V_{DS}$ → error in matching.

Solution: Put cascode

In the ~~right~~ left side image if we put NMOS cascode [NMOS is current mirror $M_1 - M_2$] we eliminate $\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})}$ term, and if we put PMOS cascode [PMOS: $M_3 - M_4$ defines N] we eliminate $(1+\lambda V_{DS})$ inside $\left[\frac{1}{(\ldots)} - \frac{1}{\sqrt{N}(\ldots)}\right]$ expression.




→ $\frac{(\ldots)}{(\ldots)}$ removed

→ $\left[\frac{1}{(\ldots)} - \frac{1}{\sqrt{N}(\ldots)}\right]$ removed

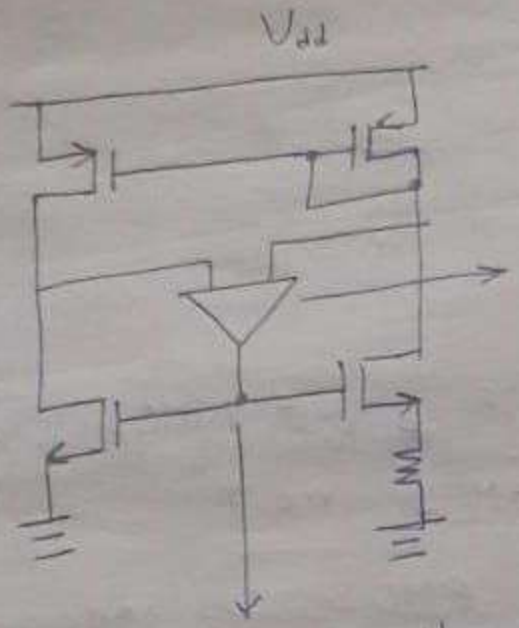
→ Process dependent (Resistor)
→ Variation is acceptable.

Drawback: More headroom, thus $V_{dd}$ ↑.

Removal of $(1+\lambda V_{DS})$ terms make current independent of supply voltage fluctuation.

$(1+\lambda V_{DS})$ → Injects $V_{dd}$ dependence

In case of precision current, we can do tunable R.

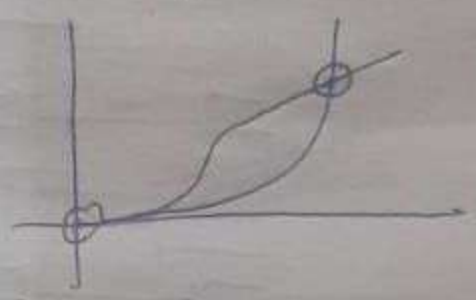



Opamp / Error amplifier
(Cost tradeoff with $V_{os}$ cancelled)

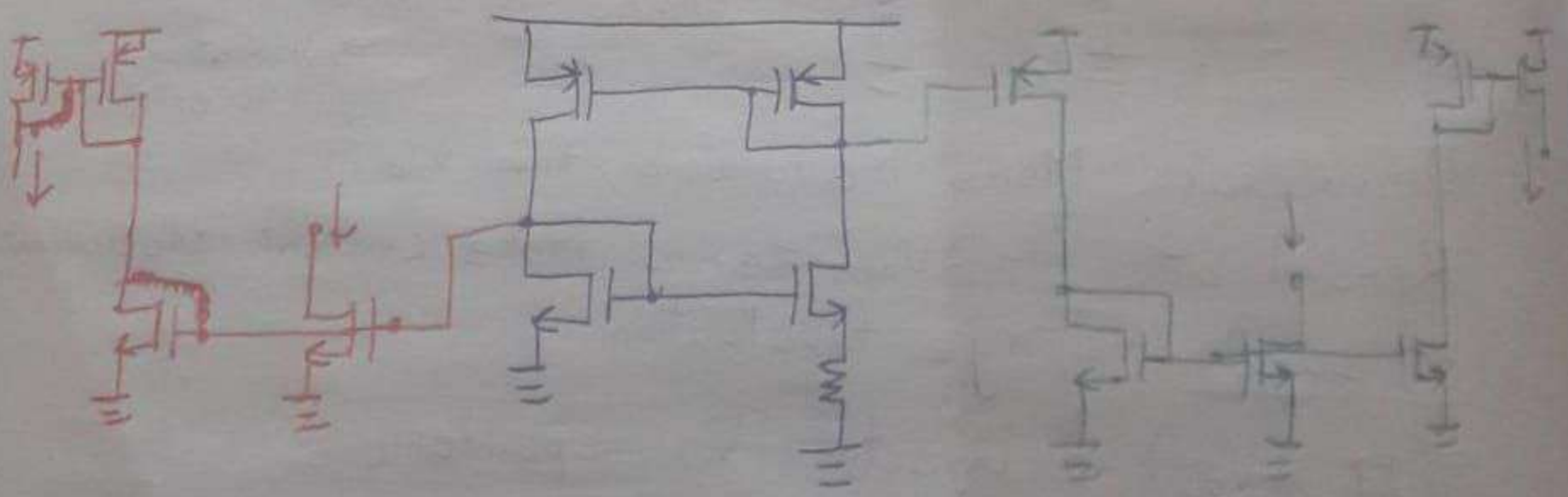
$V_G$ is monitored to cancel $\lambda V_{DS}$ terms

Basic Principle → 2 diff. characteristics
1) Square Law ($M_1$)
2) Linear + Square Law ($M_2$ + R)

We require crossing point of 2 IV curves leading to a stable point.



Utilisation of current reference in IC chips -



1 current reference is used and we can copy them infinite times throughout the circuit.

15/10/20

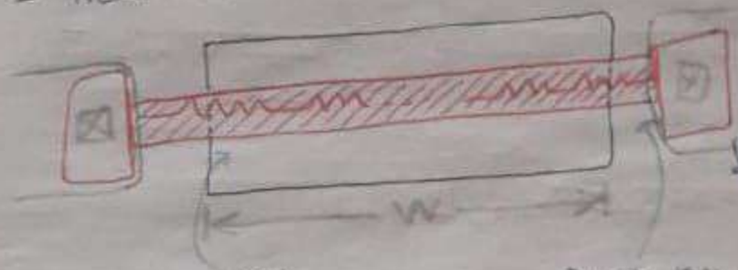
# PHYSICAL DESIGN

1)
• Issues in very wide transistor:
- Resistance in Gate layer affects speed.
- Resistance in Gate layer introduces noise

$R_S$ (Rsheet) is high

→ Distributed resistance

Poly Si 2 polymer(s) introduces more resistance



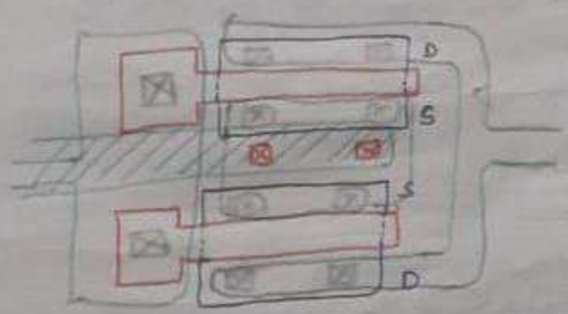

↳ Added to reduce delay [Not so eff]

Gets signal quickly

Due to res. there is delay. [Deviation in speed]

→ Prone to process Variation

• Solution – Split the transistor W>100




- Poly
- M1
- M2
- Via 1 (between M1, M2)
- Contact (Diff/Poly – M1)

Multiple element → Rectangular form (better)

[Single element → Long narrow]

0.18μ technology

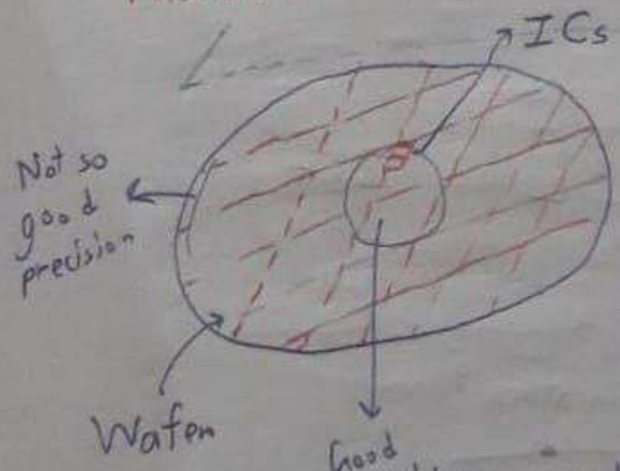
[$W_{min}$ → More imp. in digital]

$W_{min} \leq W_{element} \leq 15\mu m$

$W_{min}$: (2 to 4) $W_{min}$ → [Signal integrity]

## MATCHED PAIR TRANSISTORS

2) • Mismatch in fabrication process

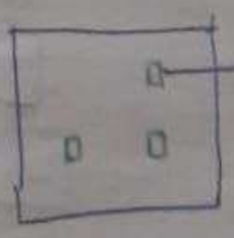



↓ Mask layer (with patterns)

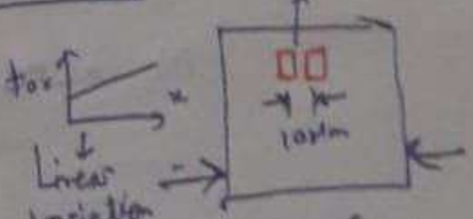
↓ Defines rectangles on the die.

One mask → 1 layer (Poly, Diff, ...)

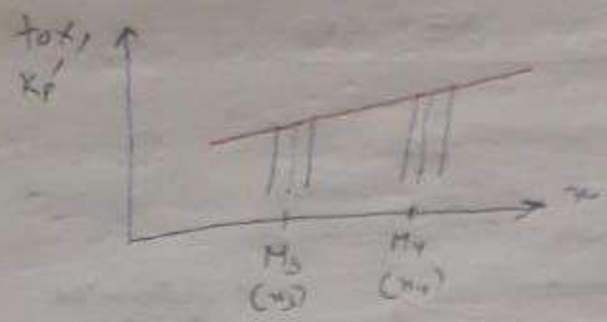
Individual die

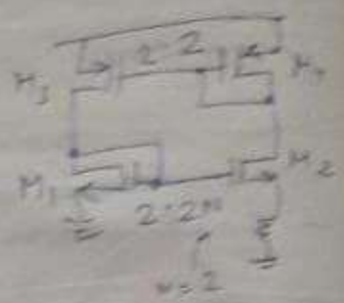



We want them to be identical



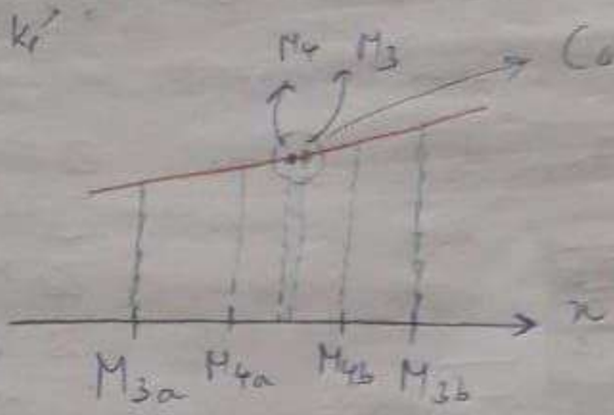

Wafer variation > Die variation



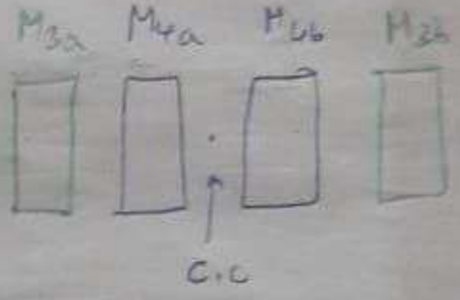

→ $M_3$, $M_4$ not identical

- Split and Common Centroid Layout




$$K_p'(M_4) = \frac{1}{2}\left[K_p'(M_{4a}) + K_p'(M_{4b})\right]$$

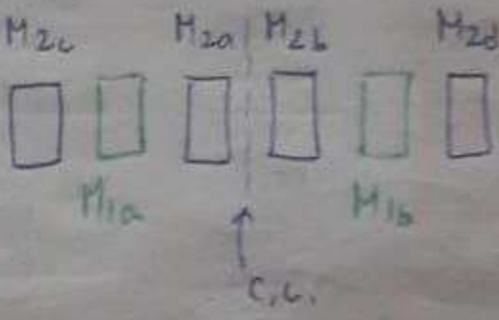
$$K_p'(M_3) = \frac{1}{2}\left[K_p'(M_{3a}) + K_p'(M_{3b})\right]$$




[2:2 matrix mentioned earlier]

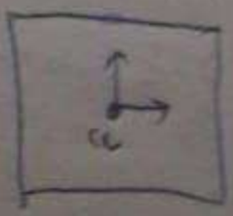
Relative variation is very small.

Absolute variation need not bother us.




2:4

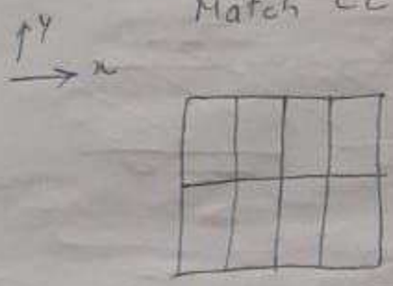
N increases → go for matrix form



What about 2D linear variation?

↳ Split into 2 orthogonal direction

Match CC in both x, y

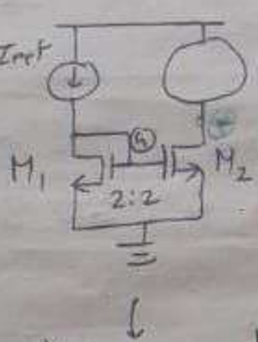


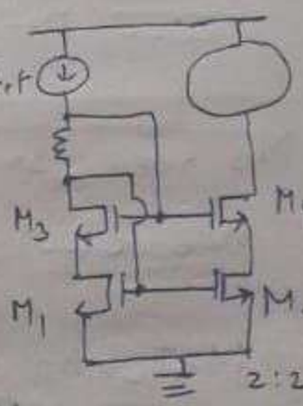
(1:1) matching?

17/10/20

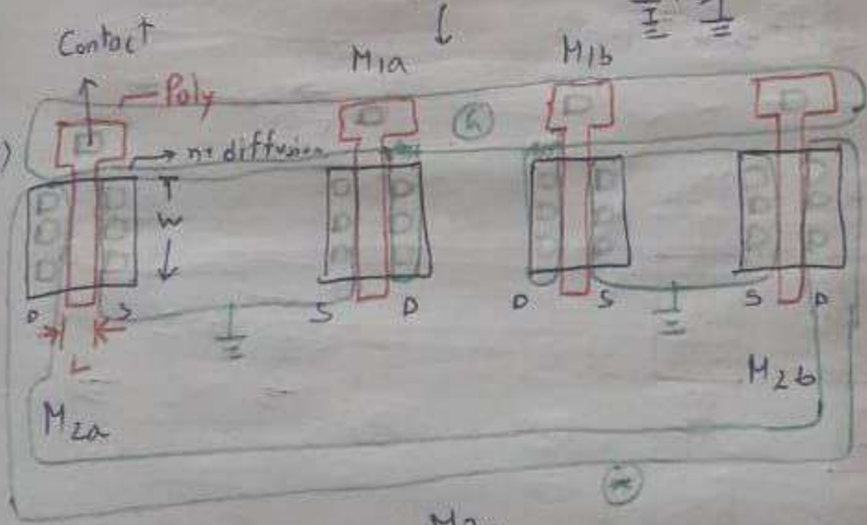
## Clustering of Matched pair transistors

- Mirror Pair (2)
- Differential Pair (2)
- Cascode Pair (3)





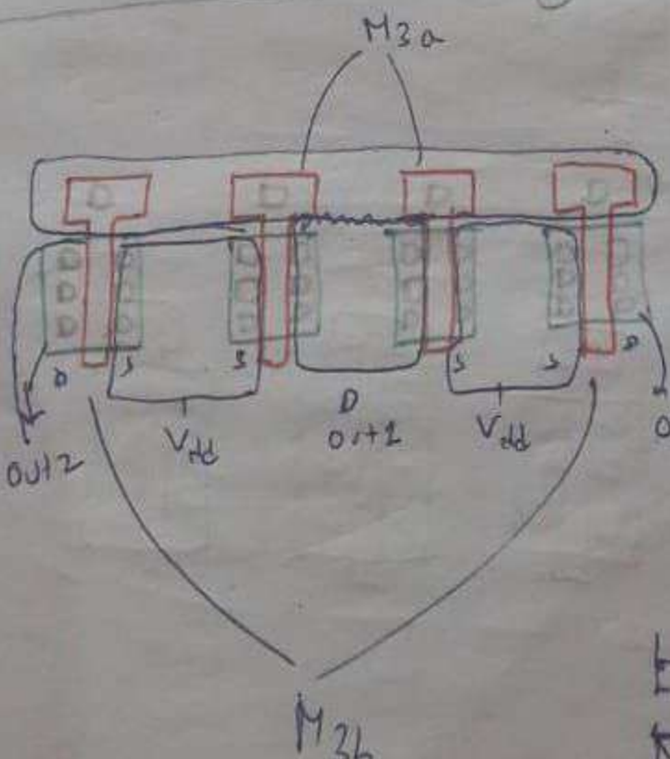

(1)



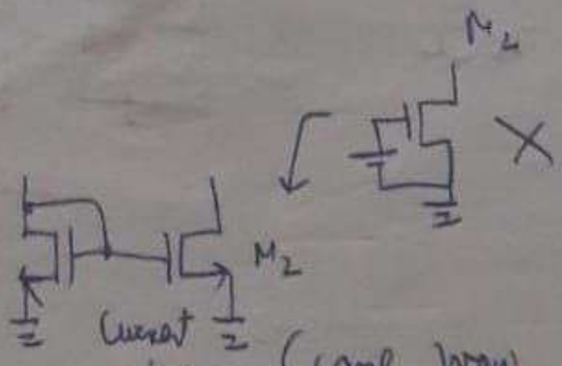

→ Mirror pair

(Almost similar to $M_{1a}, M_{1b}$ of diff. pair except GD and common gate connection

(2)



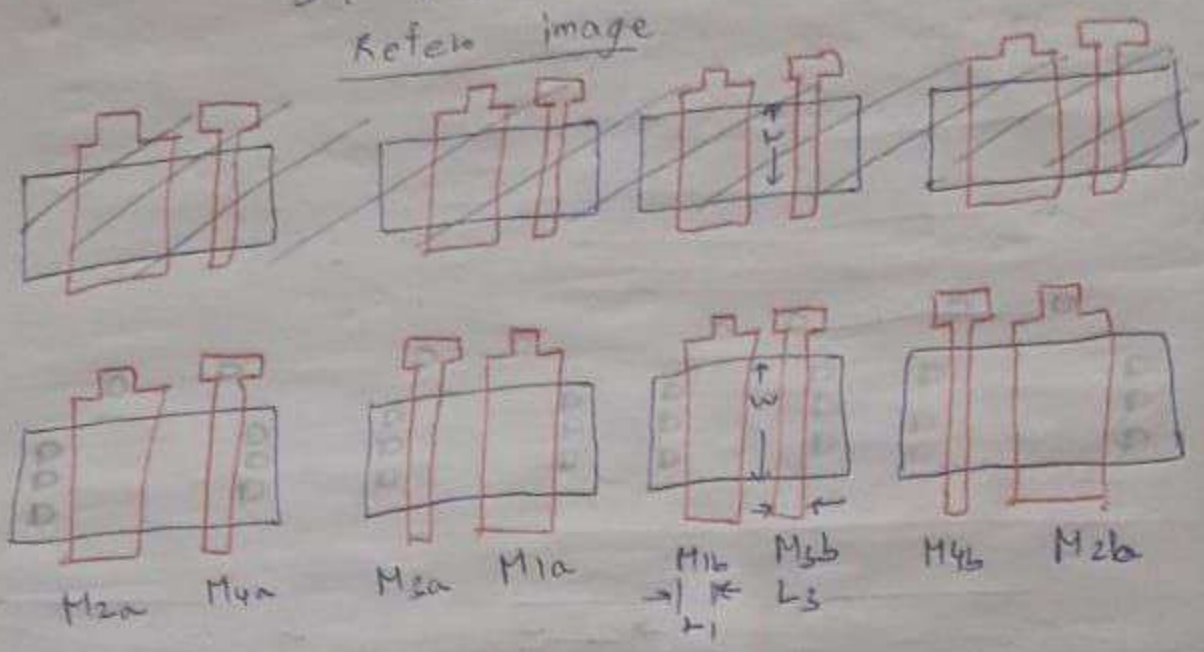

→ $M_{3a}, M_{3b}$ of diff pair

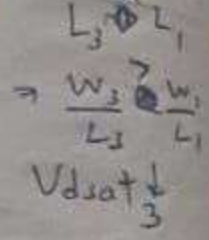



(same way)

(3) ~~B~~ S3 – D1 shorted → no contact needed
S4 – D2 shorted → no contact needed

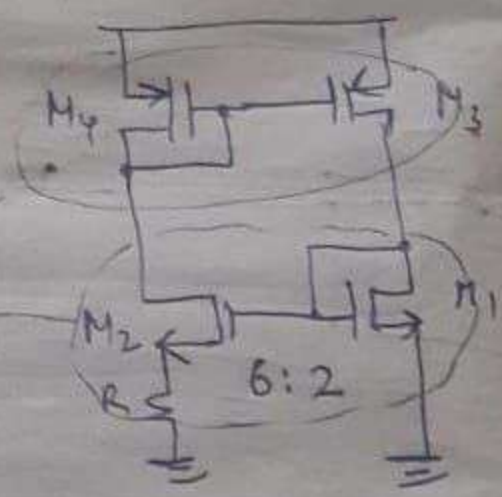
Refer image

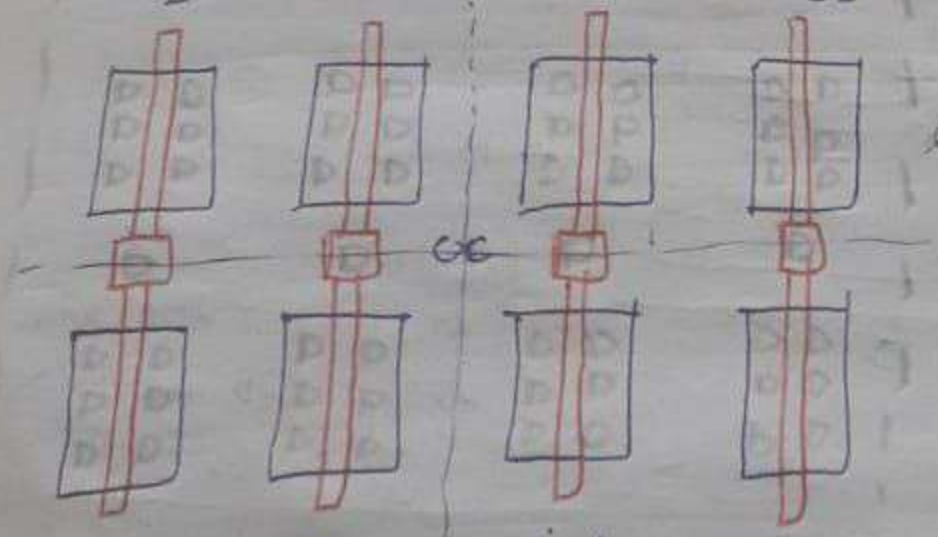


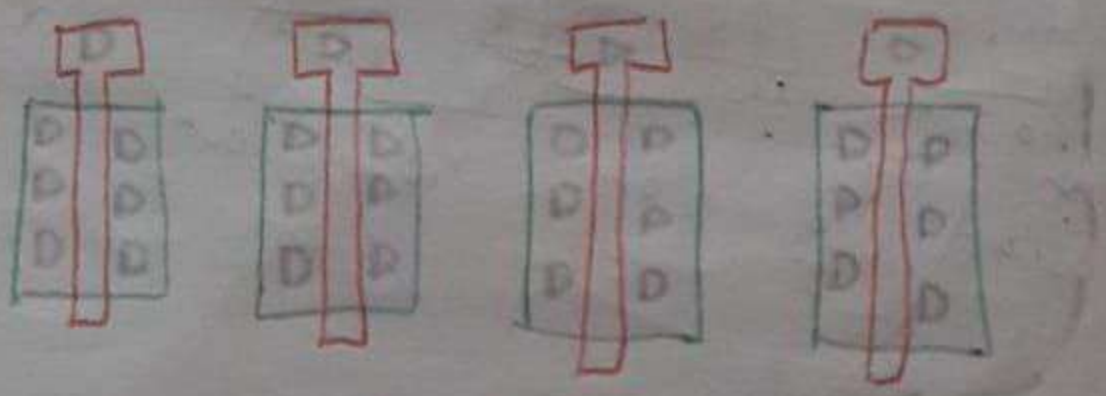

No need for seperate $M_3, M_4$ and $M_1, M_2$ matchly
We club $(M_1, M_3)$ and $(M_2, M_4)$ → Better design

- Matching with different ratios



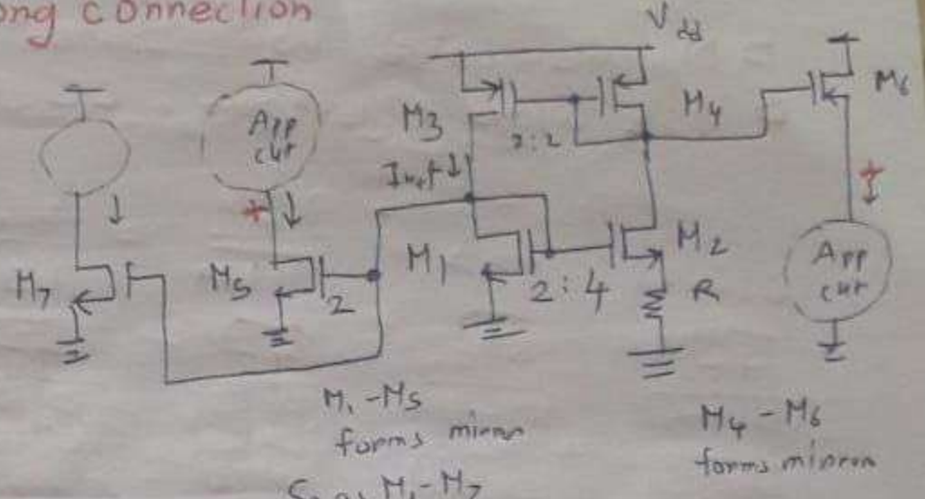

Try to keep mirroring circuit close to CC.

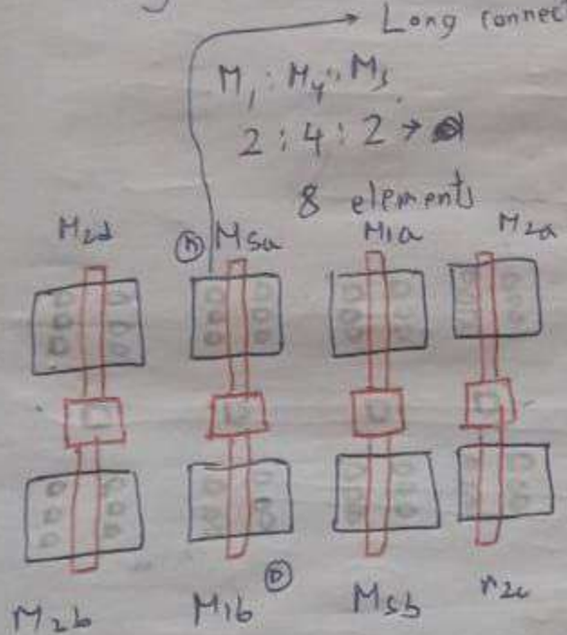


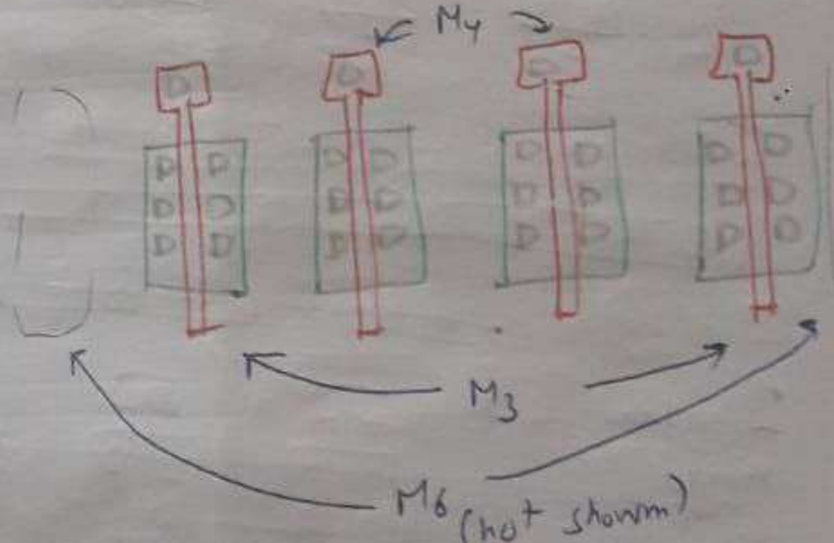
- Long connection and physical placement of cluster
- Long connection in current mode
- Shielding of a long connection

3, 4, 6 → Single cluster
1, 5, 2 → Single cluster
(Exclude 7)

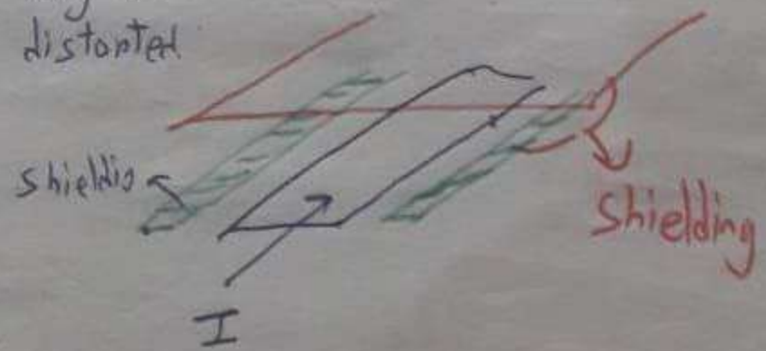
App ckts cannot be close.
But for mirror $M_5, M_1$ and $M_4, M_6$ very close.
Thus, we may have long * connection (net).



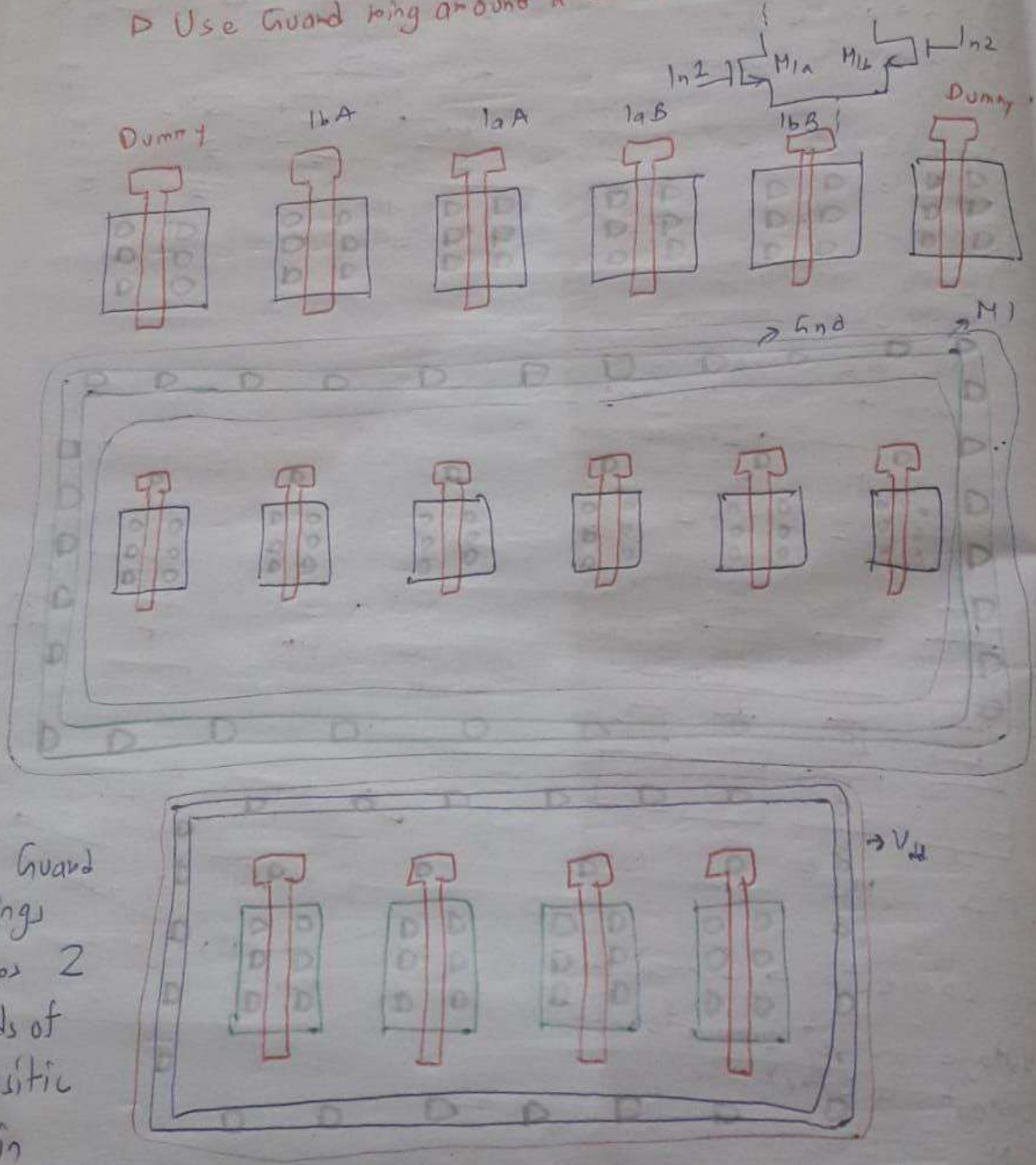




Long connection → Current mode
(Voltage can get corrupted, but current is same)
∴ $M_5$ is close to $M_1$. $V_{G1}$ is to be transferred to $V_{GS}$.
In case it is long connection Voltage gets distorted



- Use of Dummy and Substrate / n-Well connection
  - ↳ Use dummy elements at ends to match proximity
    - No dedicated body connection for each transistor
    - Use Guard ring around a CC cluster

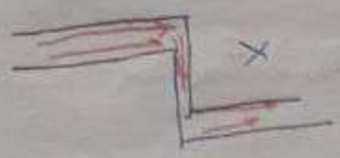



2 Guard rings stop 2 kinds of parasitic BJT in latchup circuit.

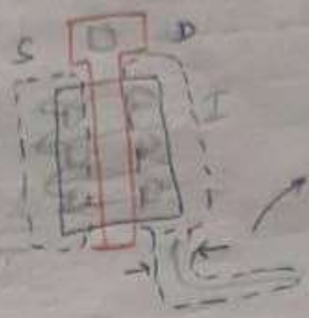
## Strong Connections

- Strong connection to support dc current

* Make sure you understand current flow connection / direction.
* Avoid current crowding



Make wide

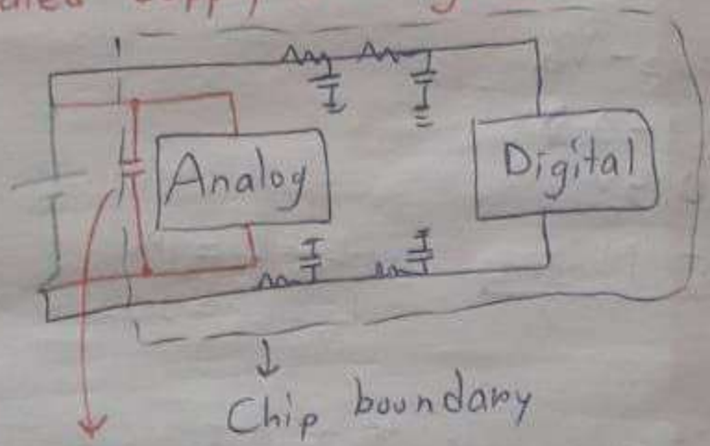



Maybe narrow for current flow

High Resistance
↳ Joule heating
→ Res ↑

With progress this metal may get thinner
↳ Destructive disconnection

- Dedicated supply and ground connections




$V_{dd}$ for analog, digital must be seperate.

22/30 - Test1 (Not good)
Highest → 28
27
26

19/10/20 (Week-8) [Qs modified]

## Simple Current Mirror

(1) $V_{ds2}$ for $I_{ds2} = 100\,\mu A$

$I_{ref} = I_{ds2} \Rightarrow V_{gs1} = V_{ds2} = V_{gs1}$

exclude it for calculation

$$100 \times 10^{-6} = \frac{100 \times 10^{-6}}{2} \times \frac{8}{1} \times (V_{gs1} - V_{th})^2 \left[1 + \lambda (V_{ds1} - V_{dsat})\right]$$

$$\Rightarrow (V_{gs1} - V_{th})^2 = \frac{1}{4} = 0.25$$

$$\Rightarrow V_{gs1} - V_{th} = 0.5 \Rightarrow V_{gs1} = 0.4 + 0.5 = 0.9\,V = V_{ds2}$$

Additional factor: $V_{DS1} - V_{dsat1}$

$= V_{GS1} - (V_{GS1} - V_{th})$

$= V_{th}$

$1 + \lambda V_{th} = 1 + \frac{0.001}{1} \times 0.4$

$= 1 + 0.004$ → Very negligible

$V_{GS1} - V_{th} = \frac{0.5V}{\sqrt{1+0.004}} = \frac{0.5}{(1.002)} = 0.499V$

Hence need not consider $(1 + \lambda V_{DS})$ factor.

(ii) $I_{DS2} = I_{ref}(1) \times \left(\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right)$

$= I_{ref} \times (1 + \lambda(V_{DS2} - V_{DS1}))$

$= 0.1 \times (1 + 0.01(1))$

$= 0.101$ mA

(iii) $V_{ds2\,min} = V_{GS2} - V_{th}$

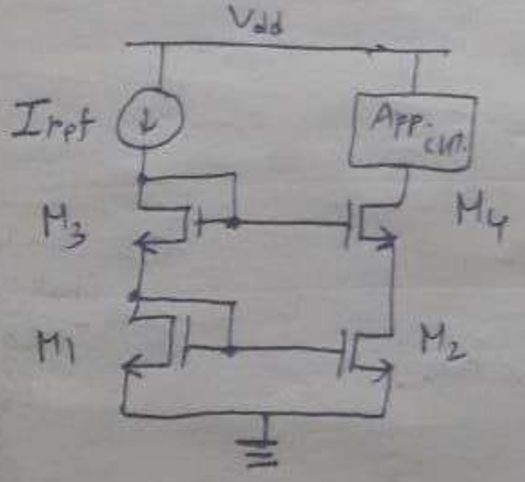
$= 0.9 - 0.4$

$= 0.5V$

## Cascode Current Mirror

$L_1 = L_2 = 1\mu m$

$L_3 = L_4 = 0.25\mu m$ → Discussed earlier




(i) $I_{ref} = I_{ds2}$

$V_{GS1} = V_{th} + \sqrt{\frac{2 I_{ref}}{K_n'(\frac{W}{L})_1}}$

$= 0.4 + 0.5$

$= 0.9$ V

$V_{GS3} = V_{th} + \sqrt{\frac{2 I_{ref}}{K_n'(\frac{W}{L})_2}}$

$= 0.4 + 0.25$

$= 0.65V$

$V_{G3} = 0.9 + 0.65$

$= 1.55$ V

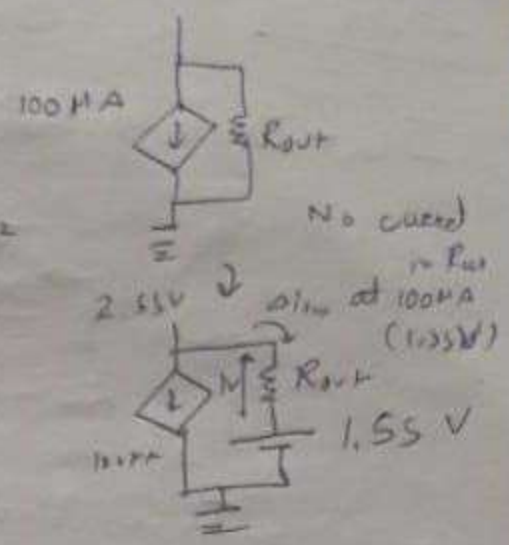
$V_{D4} = V_{D3} = V_{G3}$

$= 1.55V$

(ii) $V_{out} = V_{GS1} + 1$

$= 1.55 + 1$

$= 2.55V$




Find $R_{out}$ at D4 $\Rightarrow R_{out} = g_{m4} r_{o4} r_{o2}$

$$\Delta i_{out} = \frac{\Delta V_{out}}{R_{out}}$$

$$= \frac{1}{R_{out}}$$

$\therefore i_{out} = 100\mu A + \Delta i_{out}$

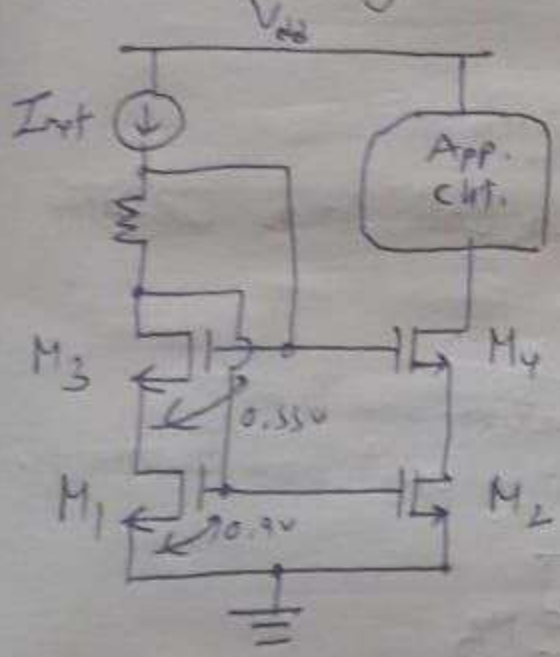
(iii) $V_{o4\,min} = V_{G4} - V_{th}$

$= V_{GS1} + V_{GS3} - V_{th}$

$= 1.55 - 0.4$

$= 1.15V$

## Wide Swing Cascode Current Mirror




(i) $I_{ds2} = I_{ref}$

$\Rightarrow V_{G4} = V_{D3}$

$= V_{GS1,2}$

$= 0.9V$

Must ensure $M_1$ and $M_2$ in sat:

$V_{GS3} - V_{th} \leq I_{ref} R \leq V_{th}$ (3 in sat)

0.25 0.3 0.4

(ii) $V_{G4} = V_{GS1} + I_{ref} R$

$= 0.9 + 0.1 \times 3$

$= 1.2$ V

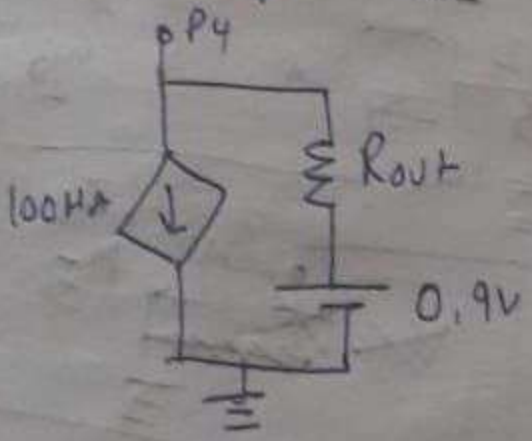
$V_{D4\,min} = V_{G4} - V_{th}$

$= 1.2 - 0.4$

$= 0.8V$

↓ Better swing.

(iii) Same as prev. (i)

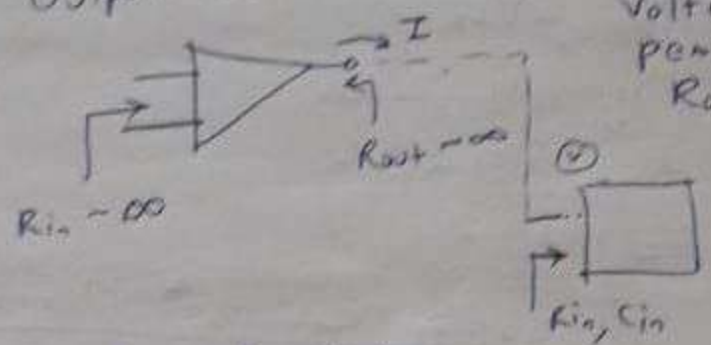


20/10/20 (Test 2 upto prev day syllabus)

# Operational Transconductance Amp (OTA)

IC-741 → Voltage operation

Transconductance amplifier
Input: Voltage (diff mode)
Output: Current




We can consider o/p as voltage but not good performance because Rout very high

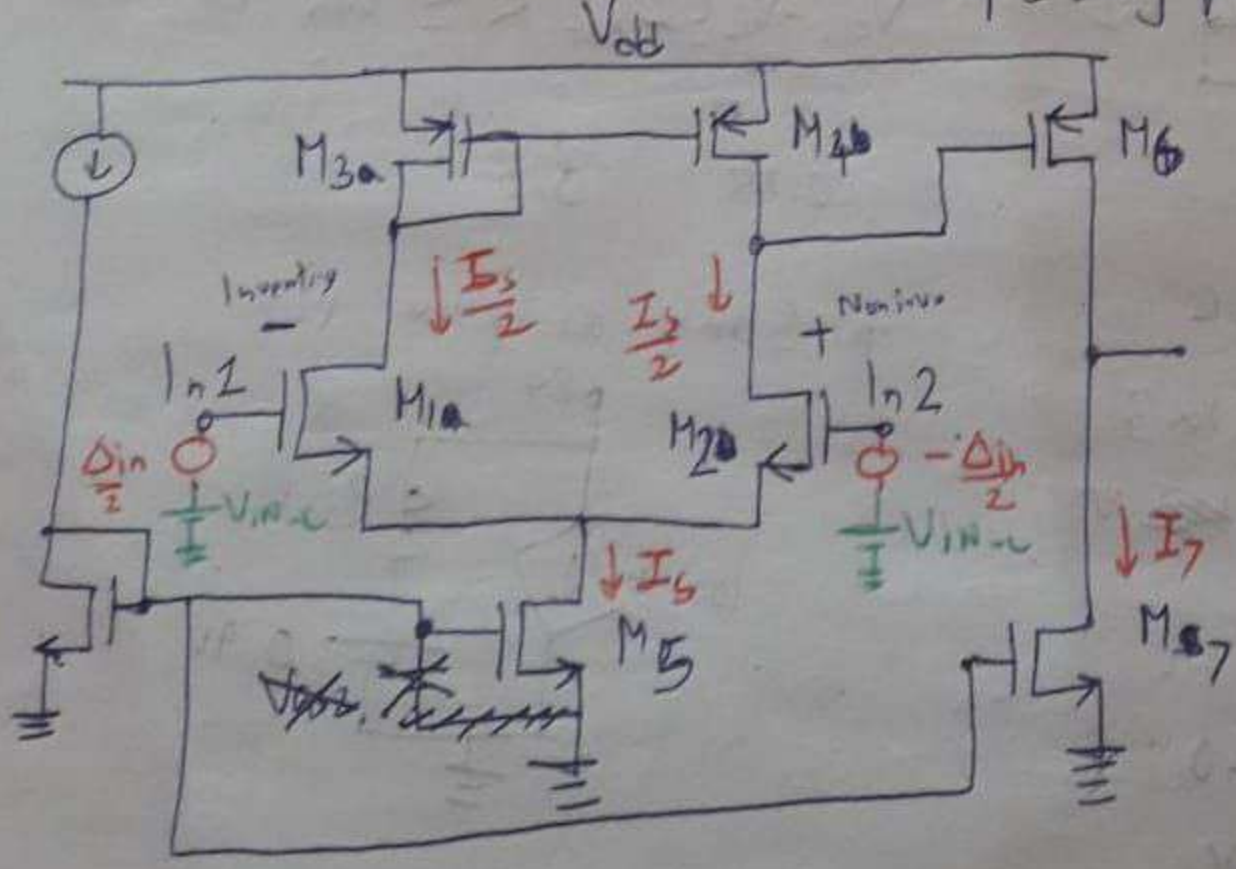
We can manage since next block is not adverse. [Suitable Rin]

In case Rin of 2nd stage cannot cope with Rout ~ ∞, we will use buffer

We will work with OTA but also call it as OP-AMP in VLSI context.

## 2 stage diff. amp.

- Construction and Biasing
- Operating point and Balance equation



(OTA)

$$A_d = \left(g_{m1}(r_{o4} \| r_{o2})\right) \times \left(g_{m6}(r_{o6} \| r_{o7})\right)$$

$$A_{CM} = \left(\frac{g_{m1}}{1 + g_{m1}(2r_{os})} \cdot \frac{1}{g_{m3}}\right) \times \left(g_{m6}(r_{o6} \| r_{o7})\right)$$

[stage 2 cannot distinguish CM, diff]

Operating point should ensure $M_6$ and $M_7$ in saturation

Current analysis:

$$\cdot I_5 = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_0} I_0 \qquad \cdot I_7 = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_0} I_0 \quad -(1)$$

Assuming quiescent conditions:

$$I_{DS1} = I_{DS2} = I_{SD3} = I_{SD4} = \frac{I_5}{2}$$

In DC: $V_{D3} = V_{G3} = V_{D4}$

$\Rightarrow$ $M_6$ indirectly forms current mirror with $M_3$ (*)

$$I_6 = \left(\frac{I_5}{2}\right) \cdot \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_3} \qquad \left[\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_3\right]$$

$$\Rightarrow I_6 = \frac{I_0}{2} \times \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_0} \times \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_{4,3}} \quad -(2)$$

Same branch $\rightarrow I_6 = I_7$ (From (1) and (2), we get)

$$\Rightarrow \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_0} = \frac{1}{2} \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_0} \times \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_{4,3}}$$

Balance equation

[It reduces offset of circuit]

$\rightarrow$ Systematic offset (no mismatch in $M_s$)

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_7 = \frac{1}{2} \cdot \frac{W_5}{L_5} \times \frac{W_6}{L_6} \times \frac{L_{4,3}}{W_{4,3}}}$$

$\rightarrow$ 1st order current equality [$M_6$, $M_7$ are in saturation]

Since we will use this circuit in feedback, we don't need DC voltage of ~~off~~ output.

If DC volt. of output is different from $\frac{V_{DD}}{2}$ by $\Delta V_{out}$, then we can refer it back to input by input offset voltage concept. [$\Delta V_{out} > 0 \rightarrow \Delta V_{in} < 0$ for compensation]

$\left(\frac{\Delta_{in}}{2}\right) \cdot A_d = \Delta_{out}$

$\Rightarrow \Delta_{in} = \frac{2\Delta_{out}}{A_d}$ [For two sided compensation]

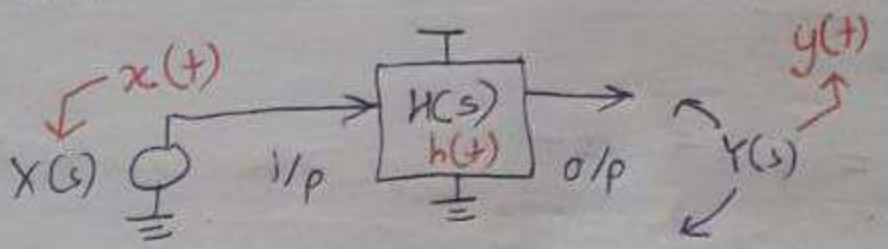
In case we go for one sided $\Delta_{in}$

$\Delta_{in} = \frac{\Delta_{out}}{A_d}$

Offset due to mismatch in transistor → Random offset
↳ (process var)

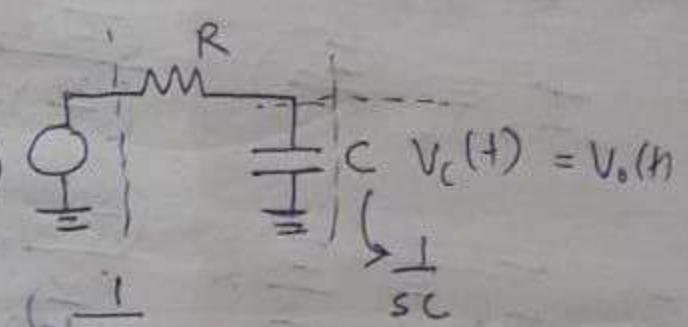
## Transfer function (Recapitulation)

- Transfer function
- Location of Poles and Zeros




$x(t) \rightarrow X(s)$

$\frac{dx(t)}{dt} \rightarrow sX(s)$




$i = \frac{dV_o}{dt} \cdot C = \frac{V_{in} - V_o}{R}$

$H(s) = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} = \frac{1}{1 + s(RC)} = \frac{N(s)}{D(s)}$

↳ $V_{in} = V_o + RC\frac{dV_o}{dt}$ → Diff. eqn. → Polynomials (Better)

Difficult

$x(t) = \sum_{i=?}^{?} w_i \, e^{s_i t}$

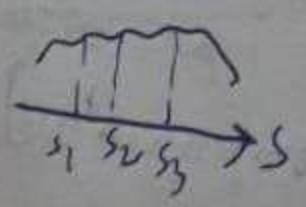
$w_i$: Weights ($X(s_i)$)

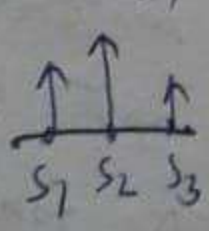
$e^{s_i t}$: Basis

The basis functions are orthogonal.

$X(s)$ → Capturing weights of basis function

$Y(s) = X(s)H(s)$ → Modulation




$\rightarrow x(t) = X(s_1)e^{s_1 t} + X_2(s_2)e^{s_2 t} + X(s_3)e^{s_3 t}$

$Y(s_1), Y(s_2), Y(s_3)$

$$y(t) = \sum_i Y(s_i)\, e^{s_i t}$$

$e^{st}$ → May be complex

$$e^{st} = e^{(\sigma + j\omega)t}$$

$$= e^{\sigma t} \cdot e^{j\omega t}$$

$e^{\sigma t}$: How amp. of basis func. grows?

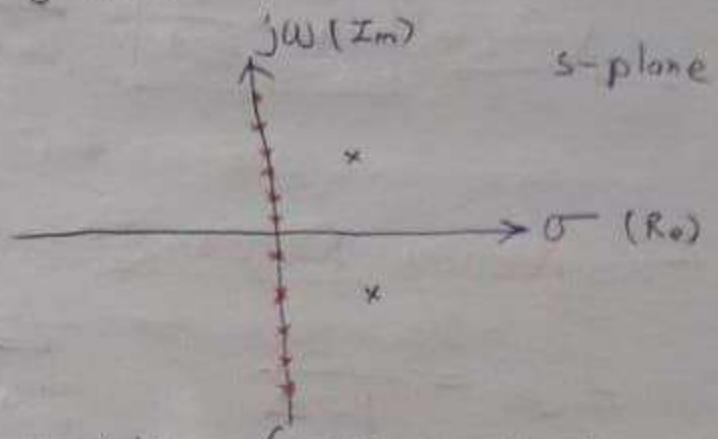
$e^{j\omega t}$: $\omega$ → How freq. signal (frequently) repeats?

For fourier transform,

$\sigma = 0$

$$H(s)\big|_{s=j\omega} = H(j\omega)$$

Each point in s-plane corresponds to a basis function




Fourier domain (behaviour in steady state)
↳ involves $j\omega$ axis only.

↳ Fourier domain

s-plane → System behaviour in transients and all conditions.

$$H(s) = \frac{N(s)}{D(s)}$$

$N(s)$ → Roots are zeroes (○)

$D(s)$ → Roots are poles (×)

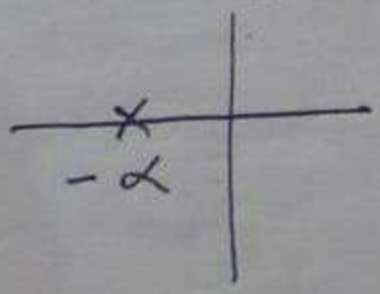
(Rational function)

System behaviour is captured by pole-zero locations.

For real systems → if we have one complex pole/zero we should have corresponding conjugate so that coefficients of TF are real → Realisable components (R, L, C are real).

Stable system → All poles lie on Left Half Plane.

Pole at real axis

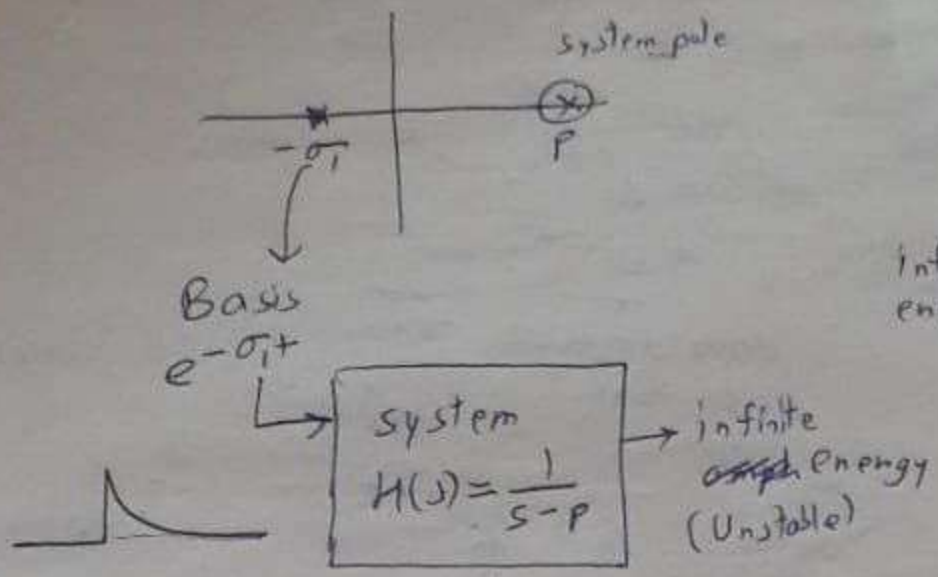


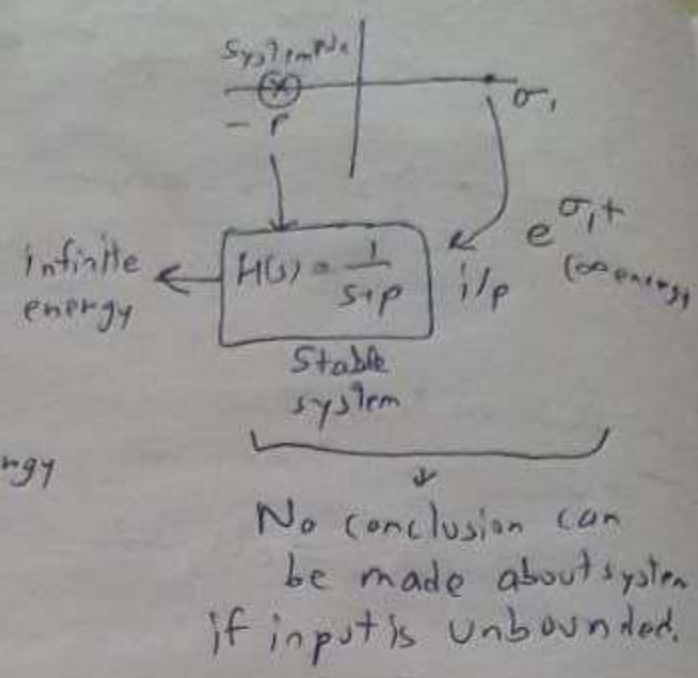

RC ckt → $\frac{1}{1+sRC}$

Pole → $s = -\frac{1}{RC}$

i/p → finite energy
o/p → finite energy
} Stable

i/p → finite energy
o/p → infinite energy
} Unstable



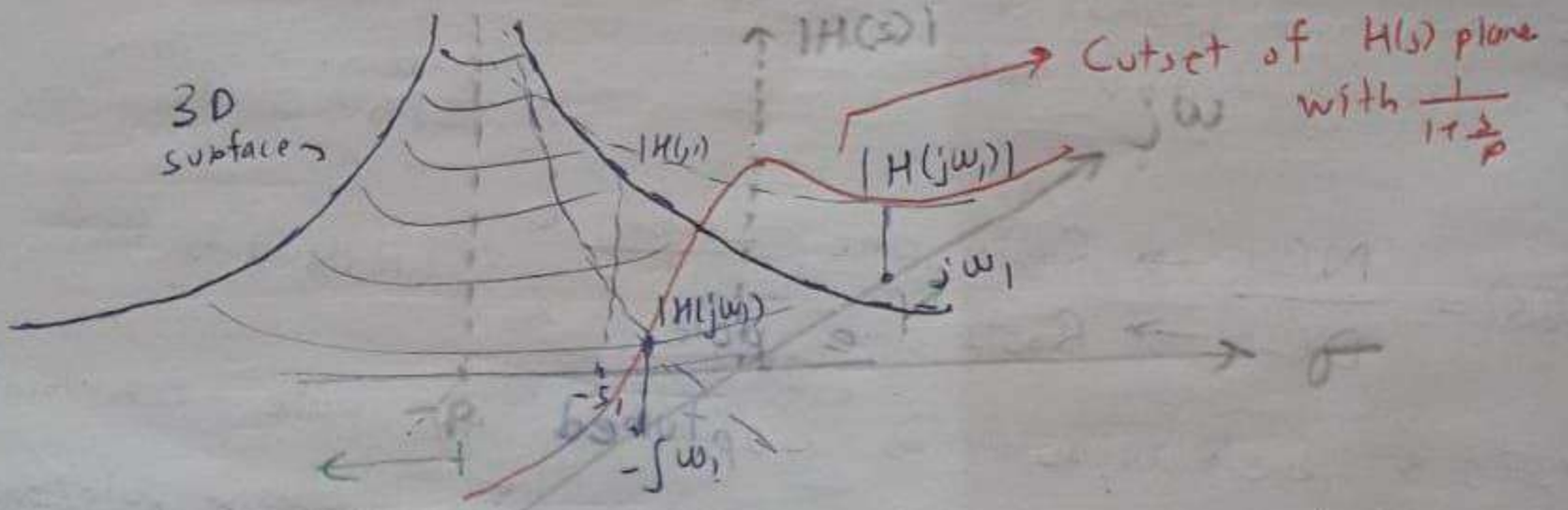




# Frequency Response

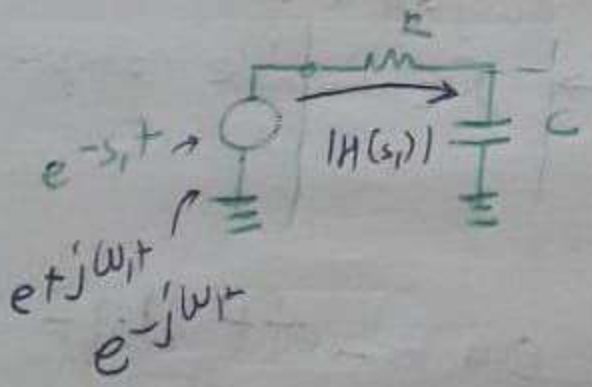
$$H(s)=\frac{1}{1+\frac{s}{p}}$$

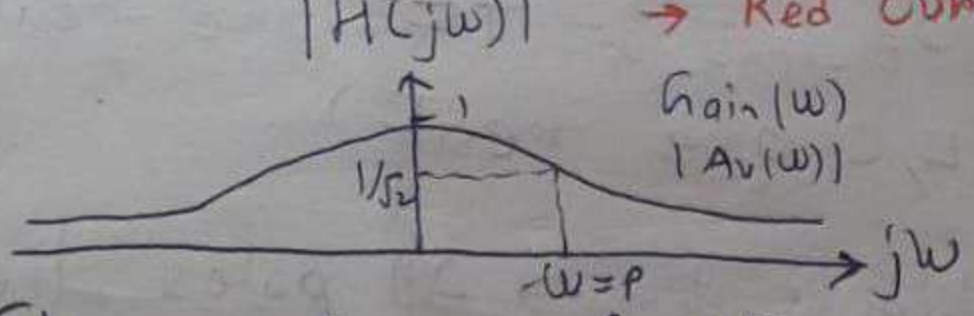
$p=\frac{1}{RC}$ → For RC ckt.

Location of the pole: $s=-p$



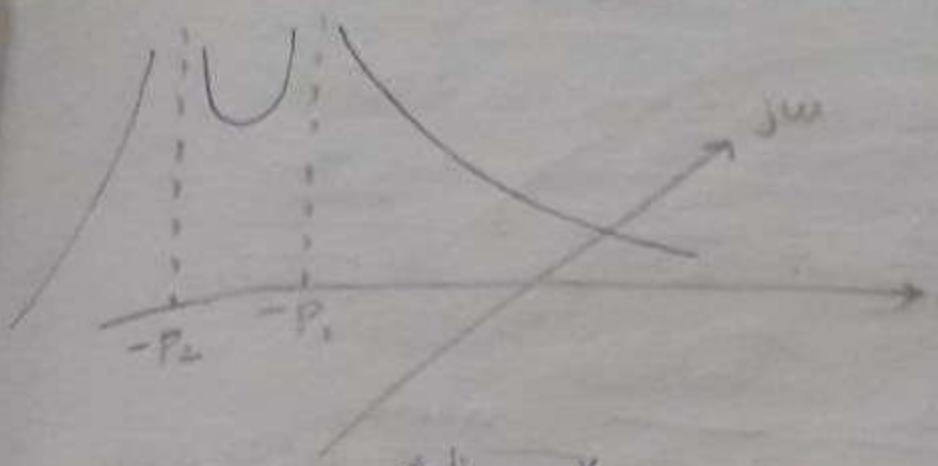

Sinusoid → $e^{j\omega t}$, $e^{-j\omega t}$ (2 con)




Pole is on $\sigma$ axis but Gain $=\frac{1}{\sqrt{2}}$.
point is an implication of this pole.

Change of gain of ckt from 0 to ∞ frequency.




$\frac{1}{(1+\frac{s}{P_1})}$ $\frac{1}{(1+\frac{s}{P_2})}$

↓

2nd order

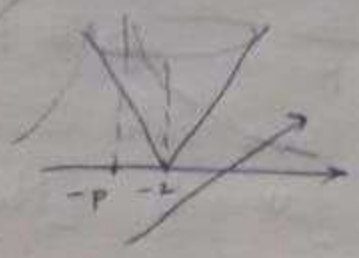
↓

Faster roll off

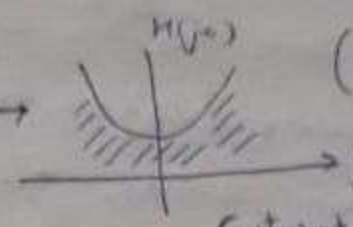
↓

Rate of roll off determines no. of pole in system

$\frac{(1+\frac{s}{Z})}{(1+\frac{s}{P})}$ → Zero




→




$(1+\frac{s}{Z})$ only

Cut-set

Move away from 0 → More amp.

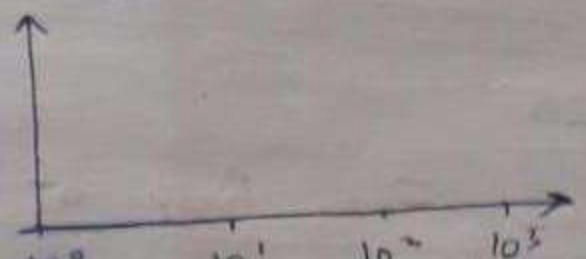
In linear scale, we cannot capture much info.

↳ Use log scale

origin cannot be seen.

[Bode plot]

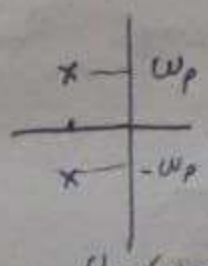
$20 \log_{10} |H(j\omega)|$

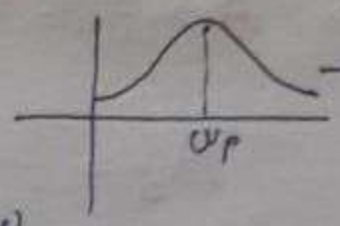



Pole at jω axis → ∞ amplitude

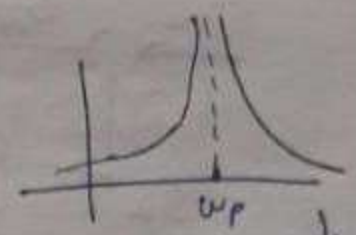
↳ Used in oscillator

$s = \pm j\omega_p$




→ Peaking (finite)




↓

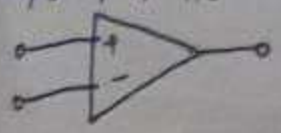
Quasi stable

0 i/p → finite o/p

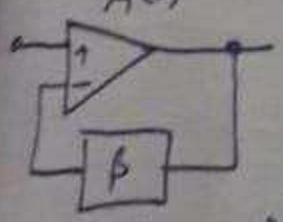
$\omega A$

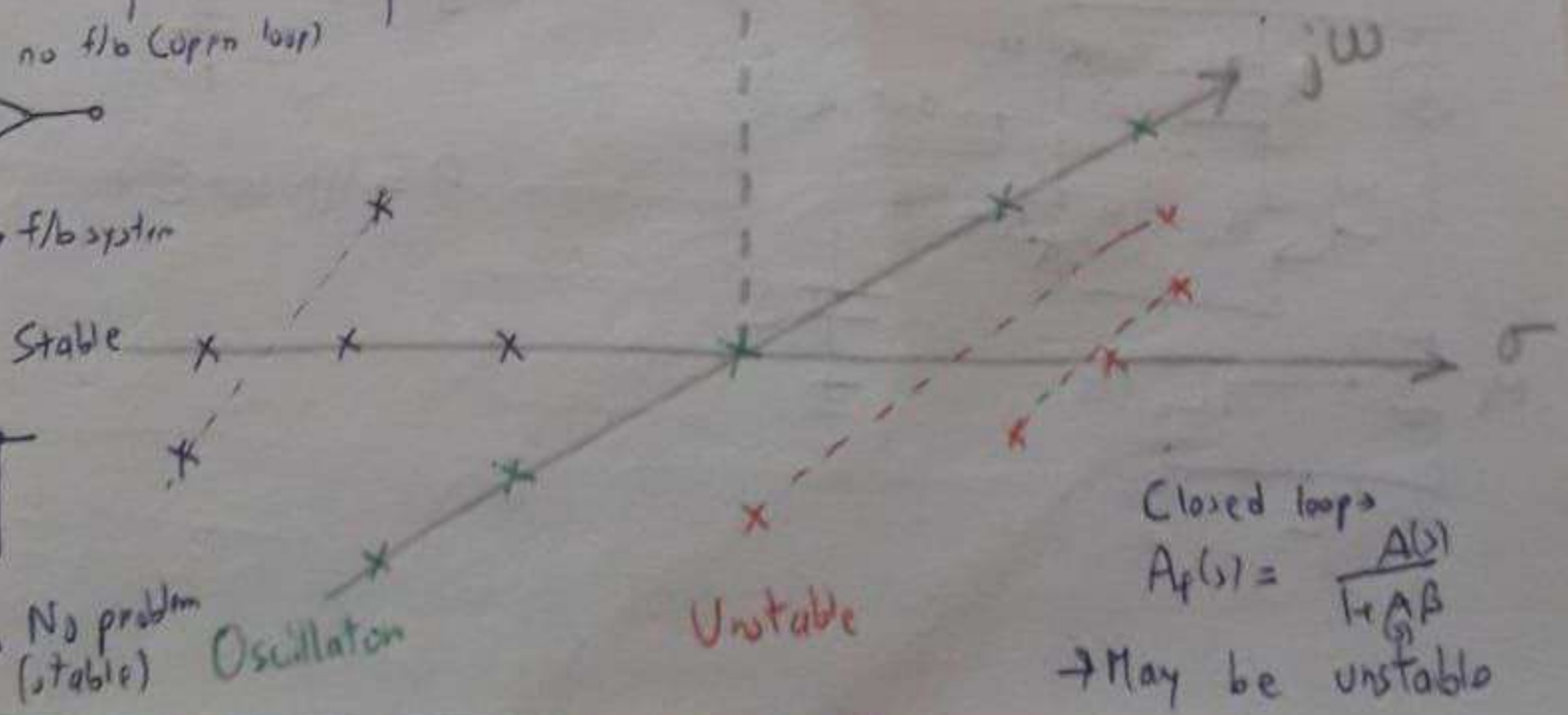
$H(s)$

$O_{pamp}$ → no f/b (open loop)



Amplifier → f/b system




$A(s) = \frac{1}{s+p}$ → No problem (stable)

Closed loop →

$A_f(s) = \frac{A(s)}{1+A\beta}$

→ May be unstable

$A(s) = \frac{A_0}{\left(1+\frac{s}{p}\right)}$ $p>0 \rightarrow$ Stable pole

We will use f/b system [investigate $A_f(s)$]

$$A_f(s) = \frac{\frac{A_0}{\left(1+\frac{s}{p}\right)}}{1+\frac{A_0\beta}{1+\frac{s}{p}}} = \frac{A_0}{A_0\beta+1+\frac{s}{p}} = \frac{\left(\frac{A_0}{A_0\beta+1}\right)}{\left(1+\frac{s}{p(1+A_0\beta)}\right)}$$

$$A_f(s) = \frac{A_0}{1+A_0\beta} \cdot \frac{1}{1+\frac{s}{p'}} \quad \text{where} \quad p' = p(1+A_0\beta)$$

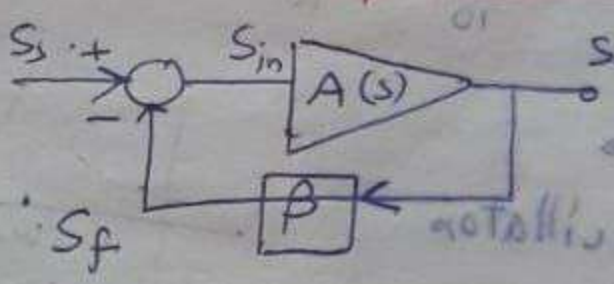
We are lucky that new pole is shifted further away from jω axis. [No stability issue]

But multiple poles → poles may collide and form conjugate pair [β can change modulation pole location].

Always ensure $A_f(s)$ is stable [A(s) must be stable].

22/10/20

## T.F and Freq. Resp of amp. in feedback config.

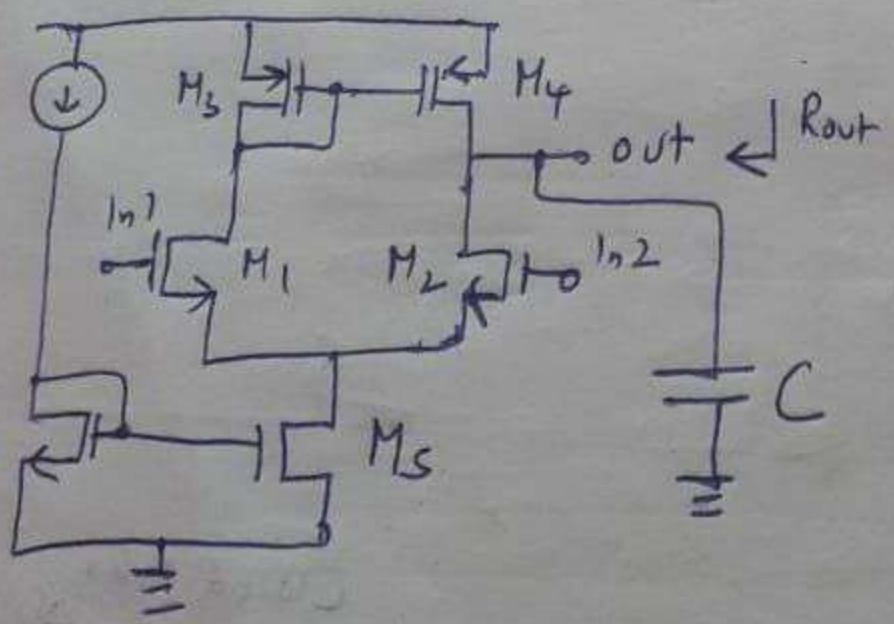



Single pole

$S_{out} = A(s) \cdot S_{in}$

$$A_f = \frac{S_{out}}{S_s} = \frac{A(s)}{1+\beta A(s)}$$

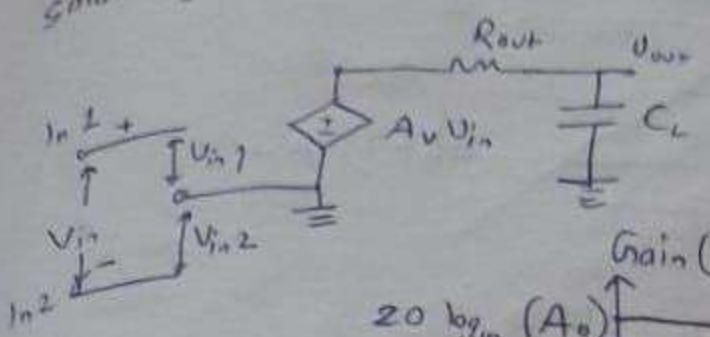
A → $A_{diff}$ of amp. ($A_d$)




$$A_d = \frac{A_0}{\left(1+\frac{s}{p}\right)}$$

$$p = 1/(R_{out}C)$$

small signal model –

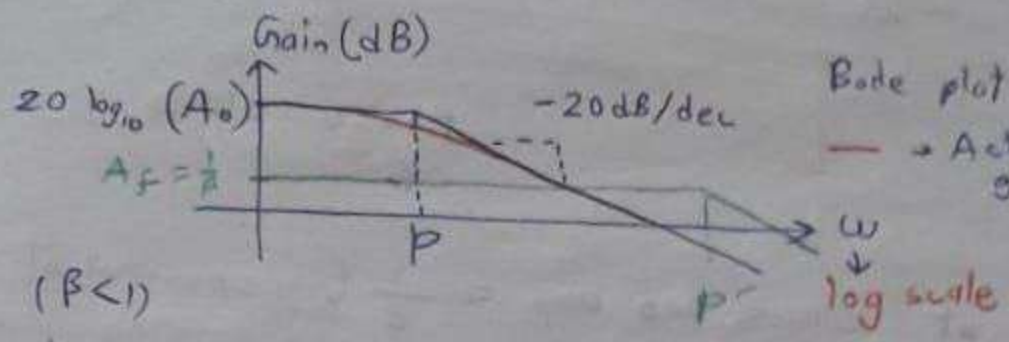



$A_v = +g_{m1} R_{out}$

($I_{n1}$ is +ve)

$\frac{V_{out}}{V_{in}} = A_d = \frac{A_0}{(1+\frac{s}{p})}$, $p = \frac{1}{R_{out} C_L}$

$R_{out} = (r_{o2} \| r_{o4})$




($\beta < 1$)

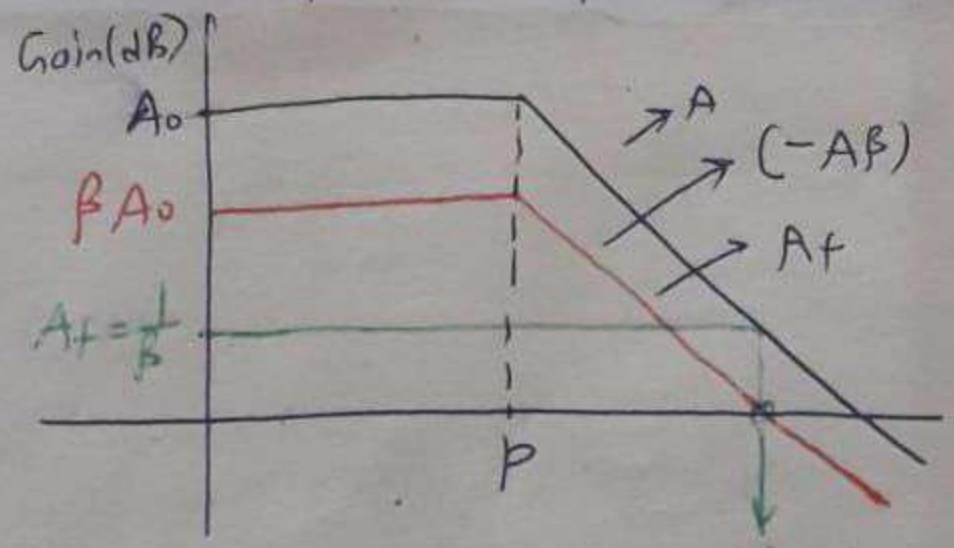
If $A_0\beta >> 1$, $A_f \simeq \frac{1}{\beta}$ [especially at low freq where $A_0$ is max]

$$A_f = \frac{A_0/(1+\frac{s}{p})}{1 + \beta A_0/(1+\frac{s}{p})}$$

$$= \frac{A_0}{1+\beta A_0 + \frac{s}{p}} = \frac{A_0}{1+A_0\beta} \cdot \left(\frac{1}{1+\frac{s}{p(A_0\beta+1)}}\right)$$

Pole of $A_f = p' = p(1+A_0\beta)$

→ $A_f$ is expected to continue as $\frac{1}{\beta}$ upto $p'$.

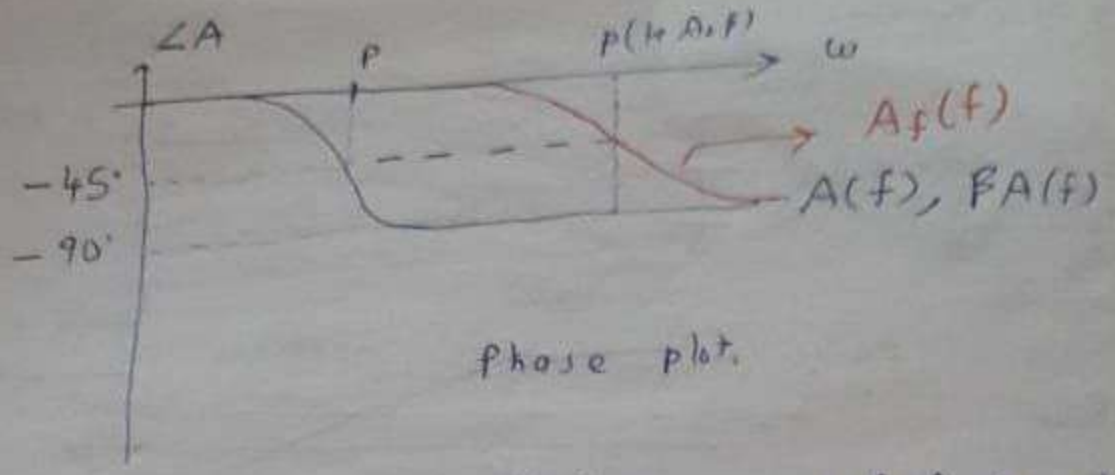



$A_f = \frac{1}{\beta}$ is valid as long as $A\beta > 1$ and i.e. upto $p' = p(1+A_0\beta)$.

$(-A\beta)$: Loop gain including mixer

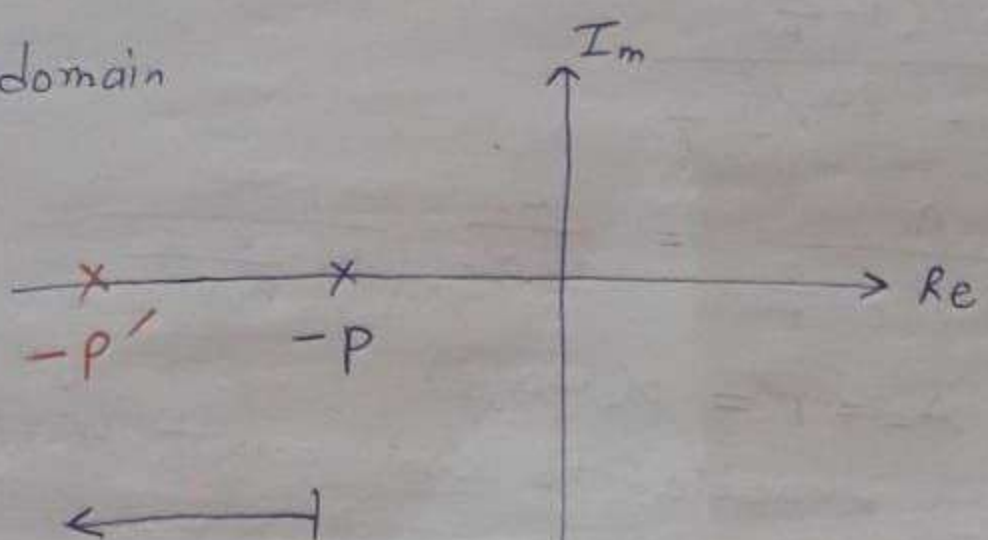
$p'$ → Unity Gain frequency

- where $A_f$ and $A_0$ become equal once again
- Loop gain $A\beta$ drops to unity




Phase plot.

Gain of closed loop amp $\approx \frac{1}{\beta}$ (independent of freq) upto BW $= \frac{1}{2\pi RC}(1+A_0\beta)$ [Bandwidth increases]




$P = \frac{1}{R_{out}C}$

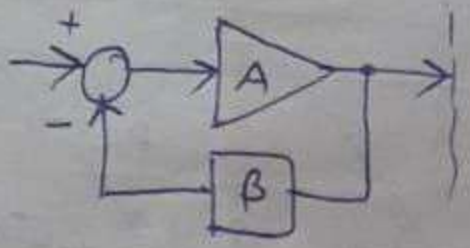
$P' = P(1+A_0\beta)$

After f/b loop

Hence f/b system remains stable for 1 pole system.

## 2-pole amplifier

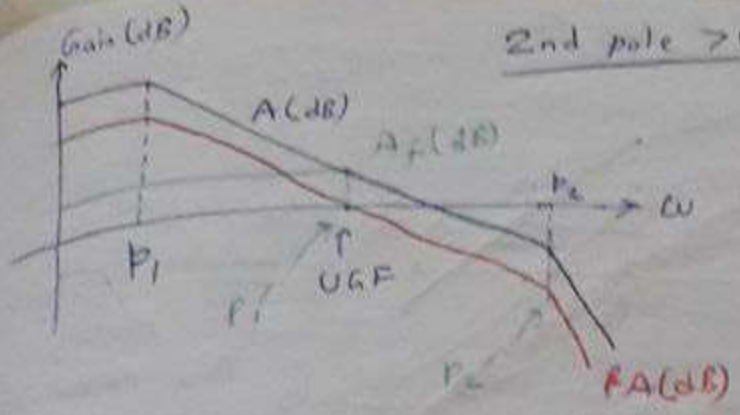
$$A = \frac{A_0}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)}$$




$$A_f = \frac{A}{1+\beta A} = \frac{\frac{A_0}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)}}{1+\frac{\beta A_0}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)}} = \frac{A_0}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)+\beta A_0}$$

$$= \frac{A_0}{\frac{s^2}{P_1P_2} + s\left(\frac{1}{P_1}+\frac{1}{P_2}\right) + 1+\beta A}$$

## 2nd pole > UGF



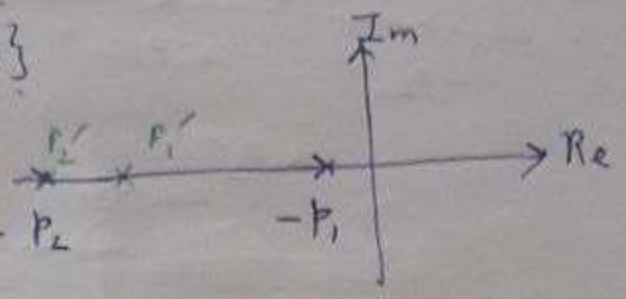

- Beyond UGF
  $A_f \approx A$

2nd pole is beyond UGF

$$= \frac{A_0}{1+\beta A_0}\left\{\frac{1}{1+\frac{s}{(1+\beta A_0)}\left(\frac{1}{P_1}+\frac{1}{P_2}\right)+\frac{s^2}{(1+\beta A_0)P_1P_2}}\right\} = \frac{A_0 f}{\left(1+\frac{s}{P_1'}\right)\left(1+\frac{s}{P_2'}\right)}$$

$$= \frac{A_0 P_1 P_2}{\{s^2 + s(P_1+P_2) + (1+\beta A_0)P_1P_2\}}$$

$P_2' = P_2 \quad P_1' = P_1(1+A_0\beta)$

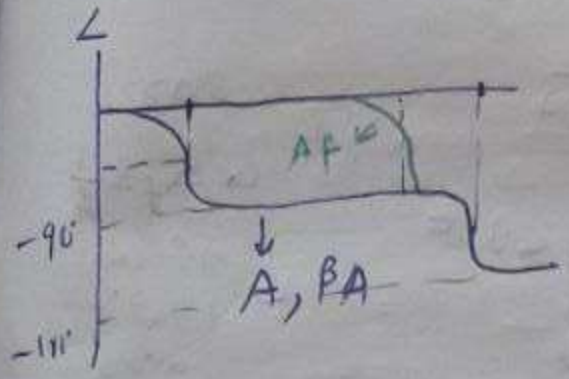



Hence f/b system is stable.

In case $P_2$ ~~is before~~ comes very close to $P_1$, the $P_1'$, $P_2'$ can clash and form complex conjugate pairs → unwanted oscillations.

$$P_1', P_2' = -\frac{(P_1+P_2)}{2} \pm \frac{\sqrt{(P_1+P_2)^2 - 4P_1P_2(1+\beta A_0)}}{2}$$

may become imaginary and cause oscillatory beh. (damped oscillation)
↳ $P_2 \leq P_1(4\beta A_0)$




$(-P_1+P_2)^2 = \sqrt{4\beta A P_1 P_2}$

$\Rightarrow P_2 = f(P_1)$

For ~~stability~~ no oscillation:

$(P_1+P_2)^2 > 4P_1P_2(1+P_0\beta)$

$P_1 << P_2$

$\Rightarrow P_2^2 > 4P_1P_2(1+A_0\beta)$

$\Rightarrow P_2 > 4P_1(1+A_0\beta) \sim 4P_1A_0\beta$

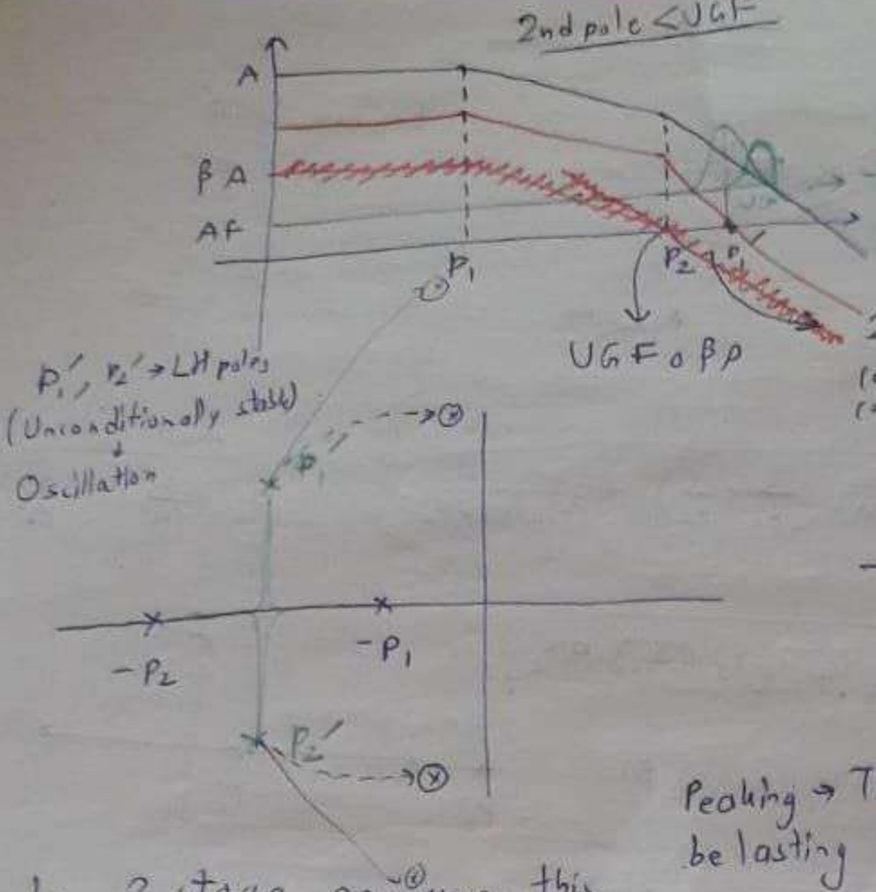
$P_1 << P_2$ ($P_1, P_2$ wide apart)

$\sqrt{P_2} = \sqrt{4\beta A P_1}$

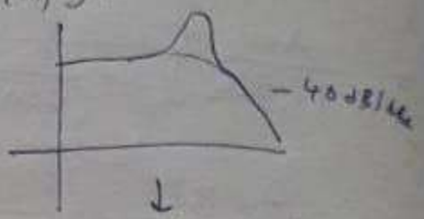
$P_2 = 4\beta A P_1$

$\boxed{P_2 > 4P_1A_0\beta}$ ~~Stable~~

To avoid oscillations




Complex conjugate poles ⇒ No intermediate roll-off




Complex conj. 2nd order freq plot

In 2 stage op-amp, this kind of behaviour can be seen. $P_1, P_2$ are close

Peaking → That freq will be lasting in the loop

If 3rd pole → that may make the system unstable.

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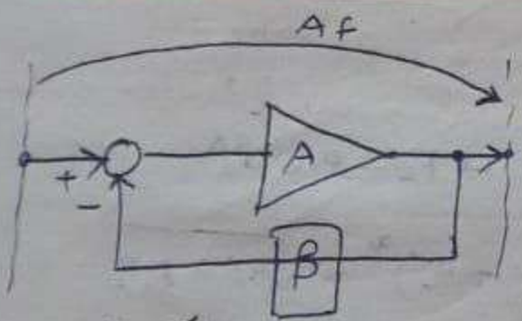
Week-9 (29/10/20)

## STABILITY ISSUE OF OP-AMP




$$A_f = \frac{A}{1+\beta A}$$

3 pole amp.

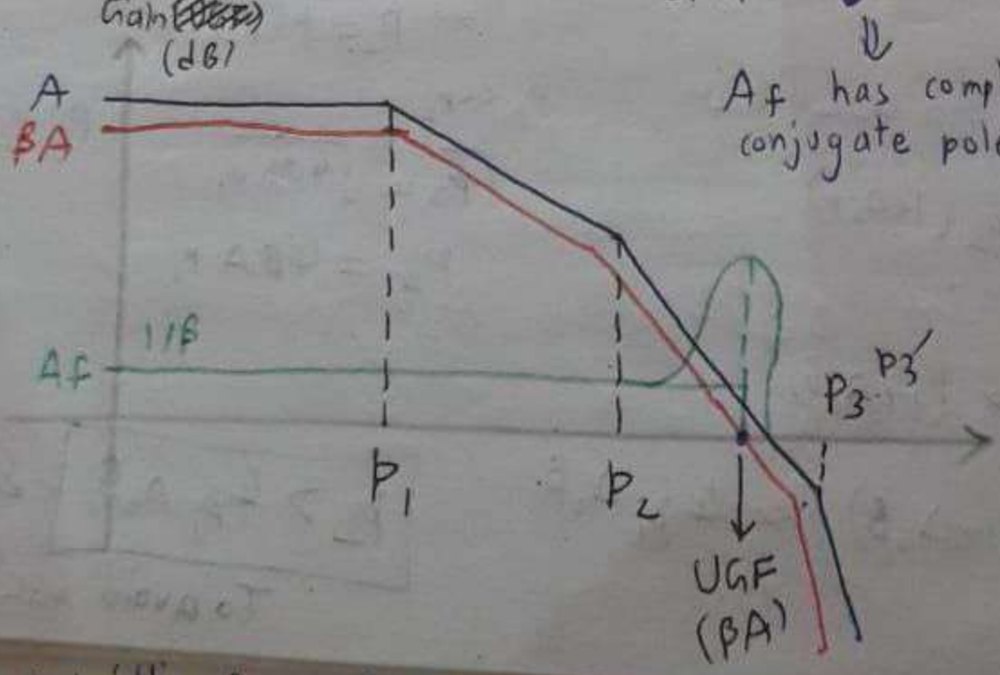
$\beta A \gg 1$

$\hookrightarrow A_f = \frac{1}{\beta}$

After that it drops (UGF)

After UGF, Af starts dropping.

2nd pole < UGF of A ⇓ Af has complex conjugate poles



Below UGF → $A_f \approx \frac{1}{\beta}$

At UGF → Complex conjugate poles $(P_1', P_2')$

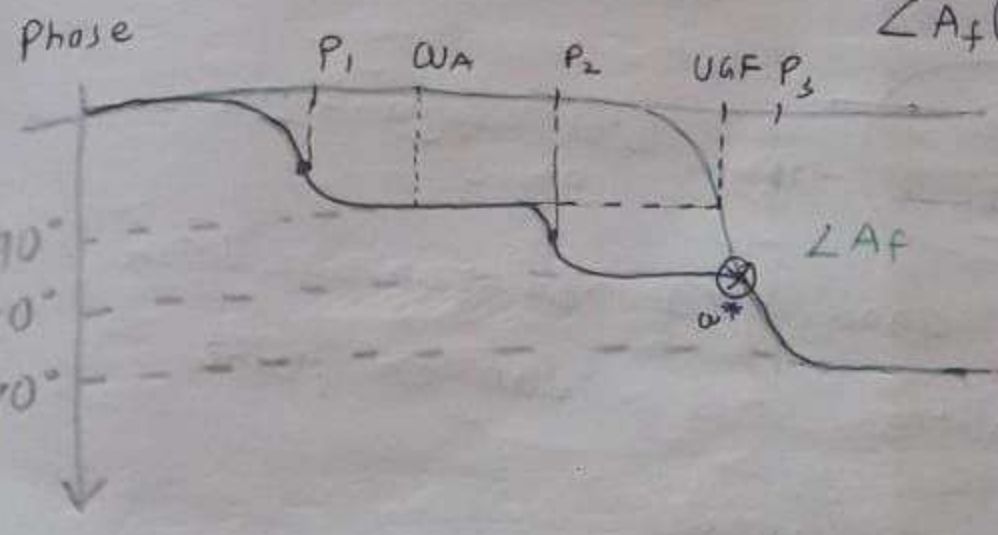
High kink ∩ in $A_f$

As $P_3$ is far apart, it remains same $P_3' = P_3$

↳ After kink, it follows A.

$$Re(P_1') = Re(P_2') = -\left(\frac{P_1+P_2}{2}\right)$$

$$\angle A_f(UGF) = -90°$$




$\omega^*$ → Phase Crossover freq.

$\omega^* = \sqrt{P_2 P_3}$

$P_2, P_3$ are equidistant from UGF

$\omega = P_1 \rightarrow \angle A\beta = 45°$

$\omega = P_2 \rightarrow \angle A\beta = 135°$

~~$\angle \beta A_{P_2} = -135°$~~ $\angle \beta A_{P_3} = -225°$ $\therefore \angle \beta A_{\omega^*} = -180°$

$\omega^* = \sqrt{P_2 P_3}$

At $\omega^*$, $\angle \beta A = -180°$, $|\beta A| = 1$

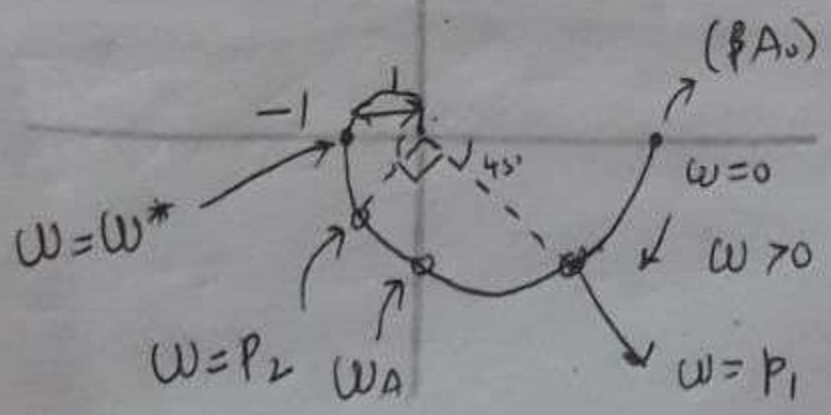
OR

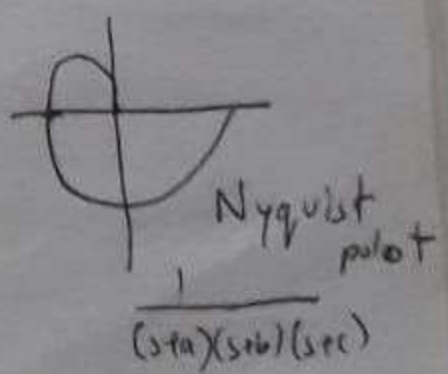
$\beta A = -1$

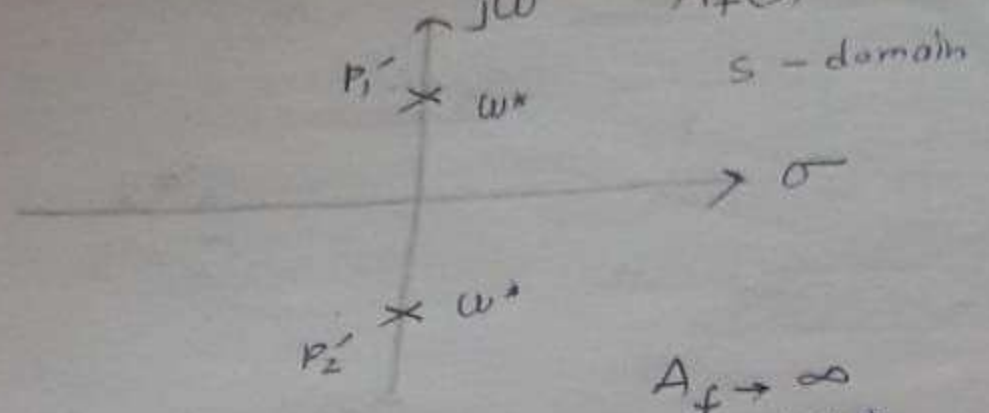
$A_f = \frac{A}{1+\beta A} \rightarrow \infty$

$\omega > P_1 \rightarrow \beta A$ starts dropping

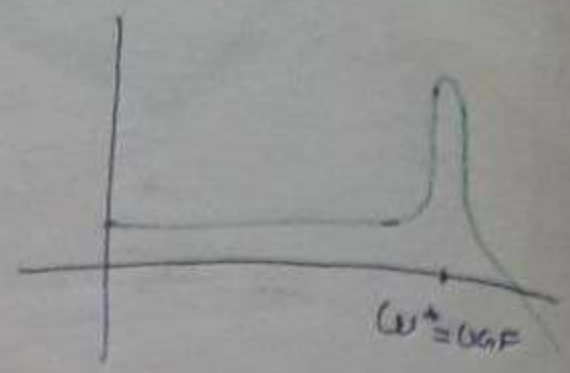
$\Rightarrow P_2, P_3$ lie on $j\omega$ axis






$A_f(s)$
s - domain




$A_f \to \infty$ at $\omega^*$

Without giving signal we get finite signal.

↓

Barkhausen criteria

At $\omega^*$

$\angle \beta A = -180°$

$|\beta A| = 1$



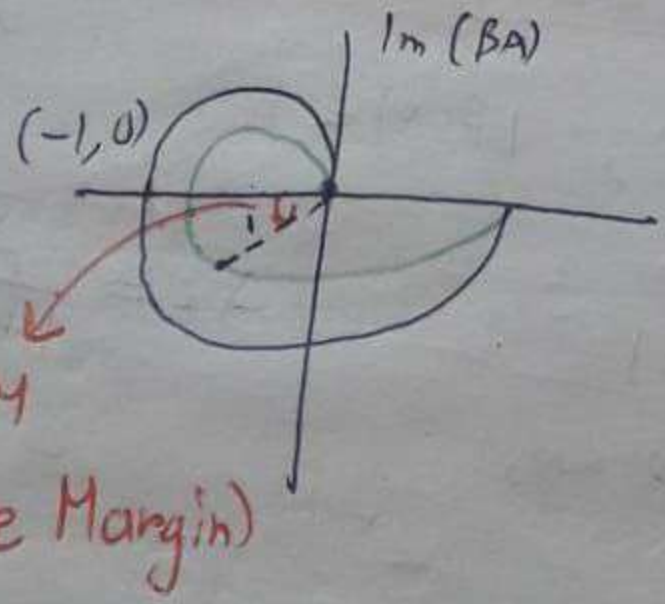

Total loop gain = $2\pi$ or $-360°$ angle

This is good / required for oscillators.

But for amplifier, it is a danger point.

How to change / avoid?

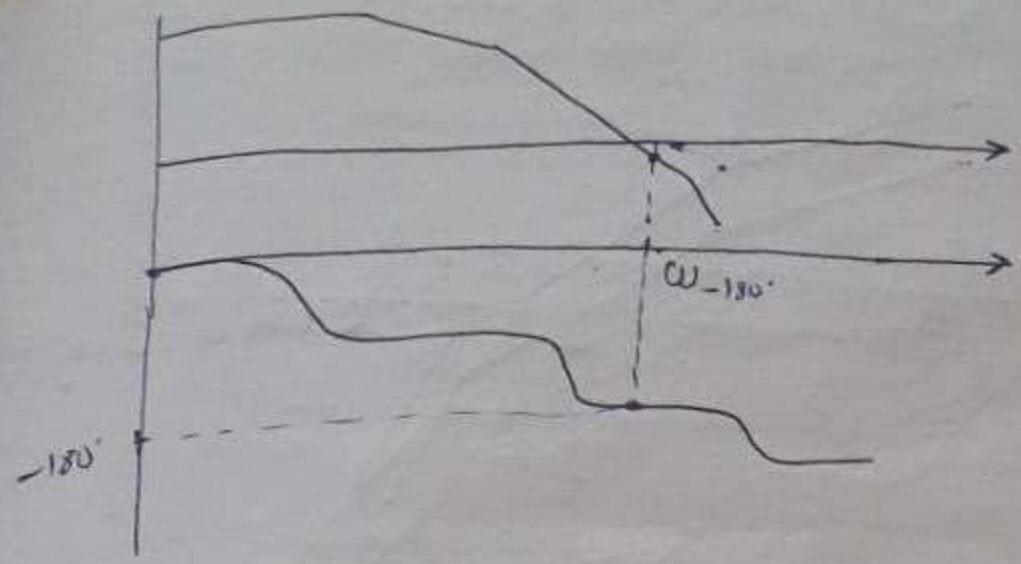
1) A can't be changed




— Reduce β → Safe

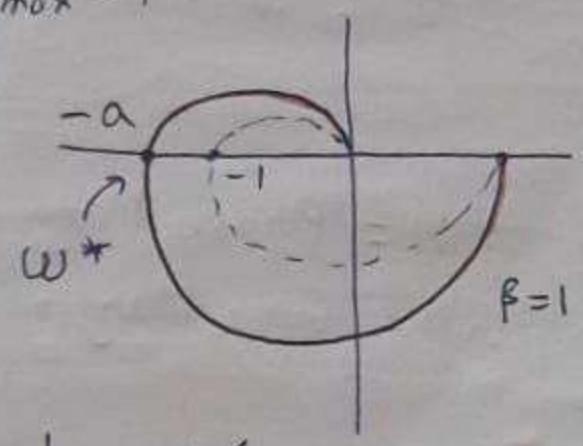
$180° + \angle \beta A|_{\omega = G_x} = PM$

$\omega = G_x$ → Unity gain frequency




At $\omega_{-180^\circ}$, the gain of loop is less than 1 and hence we don't have signal building up.
[Stable]

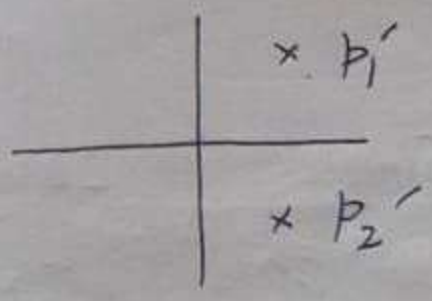
If $\beta = \beta_{max} = 1$



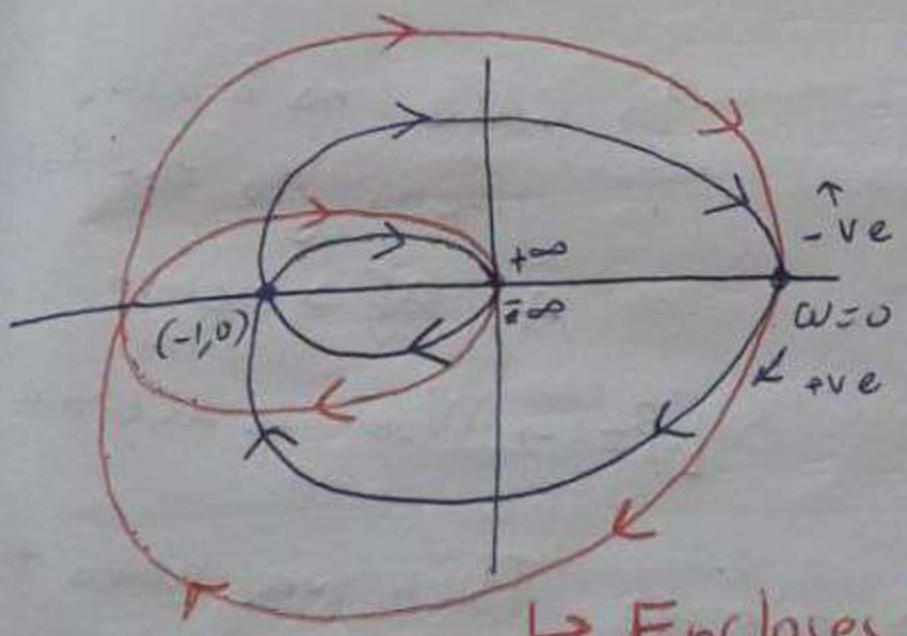

$|a| > 1$

At $\omega = \omega^*$, signal will grow up with time (even if we apply signal for small time) and output becomes $\infty$ energy.

$\Rightarrow$ The poles enter RHP




If Nyquist plot also encloses danger point $(-1,0)$ for multiple/single time that will make the system unstable



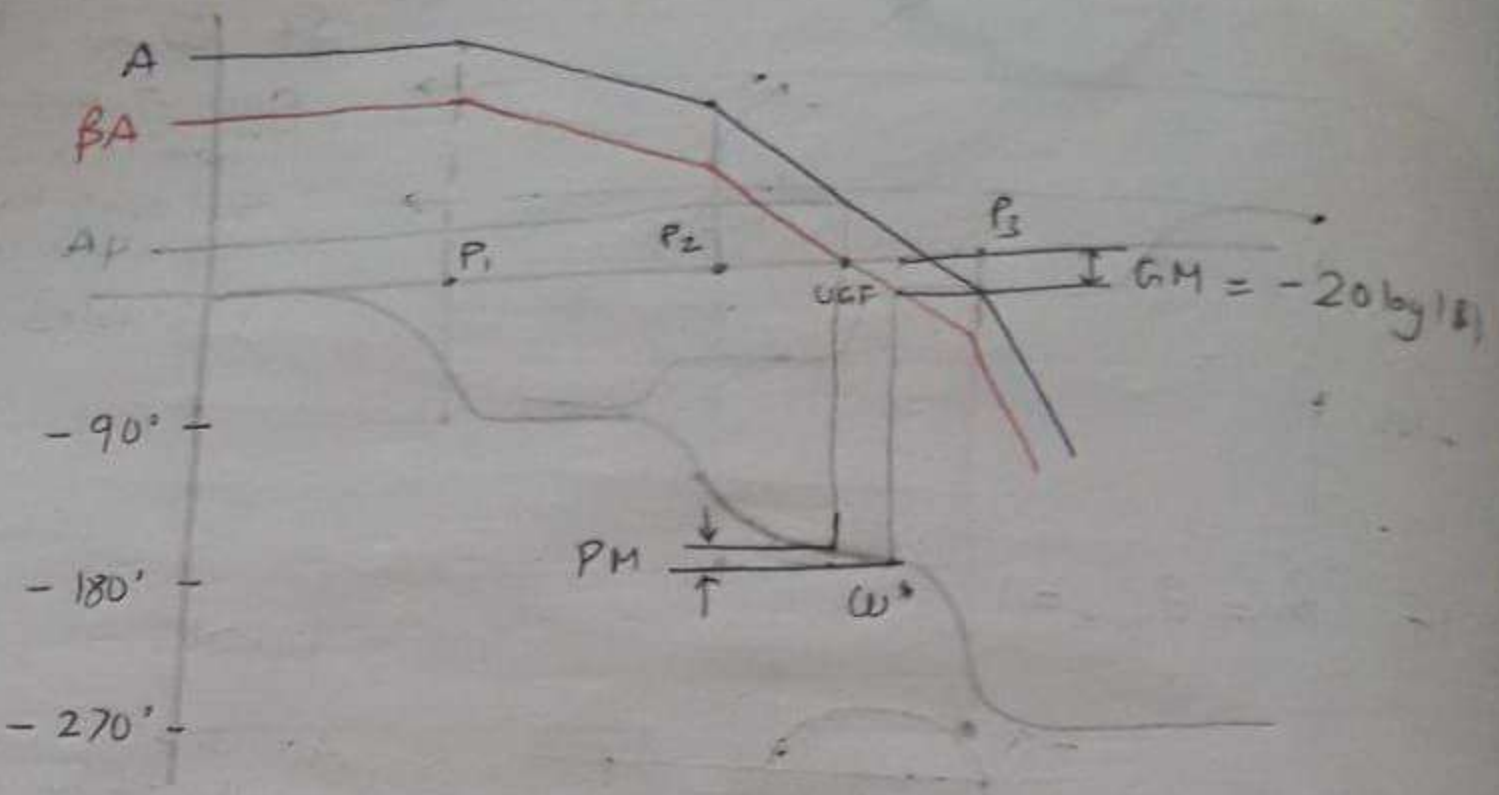

$-\infty \to 0 \to \infty$

COMPLETE NYQUIST PLOT

↳ Encloses $(-1,0)$ [Unstable]

If we have nyquist plot which encloses $(-1,0)$ atleast once, it is good enough to say that system is unstable.

# Stability Measurement of OP-AMP




PM = Phase Margin

GM = Gain Margin

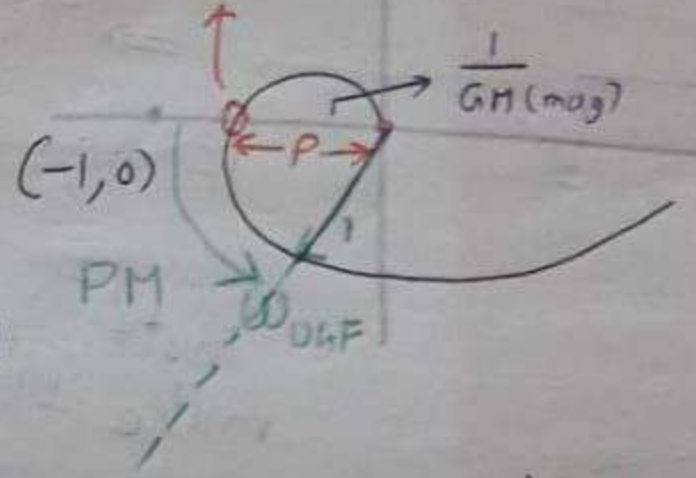
$\omega^* = \sqrt{p_2 p_3}$

PM ≥ 60° (Typical req^mt.)

Too high PM ↓

Slow system

[PM - Bandwidth tradeoff]




$\omega^*$

$|\beta| < 1$

$\therefore 20\log|\beta| = -x$

GM = x dB

If no 3rd pole ↓ $\omega^* = \infty$

No way of satisfying Barkhausen criteria.

In case no β value is given, go for β=1.

A, Aβ → merge.

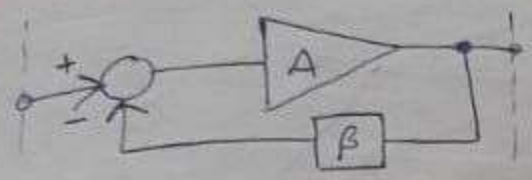
[β=1 → Worst case scenario]

β may have freq. dependence. Then we need to take poles of β into account.

31/10/20

# Stability issue of op-amp (in feedback config.)

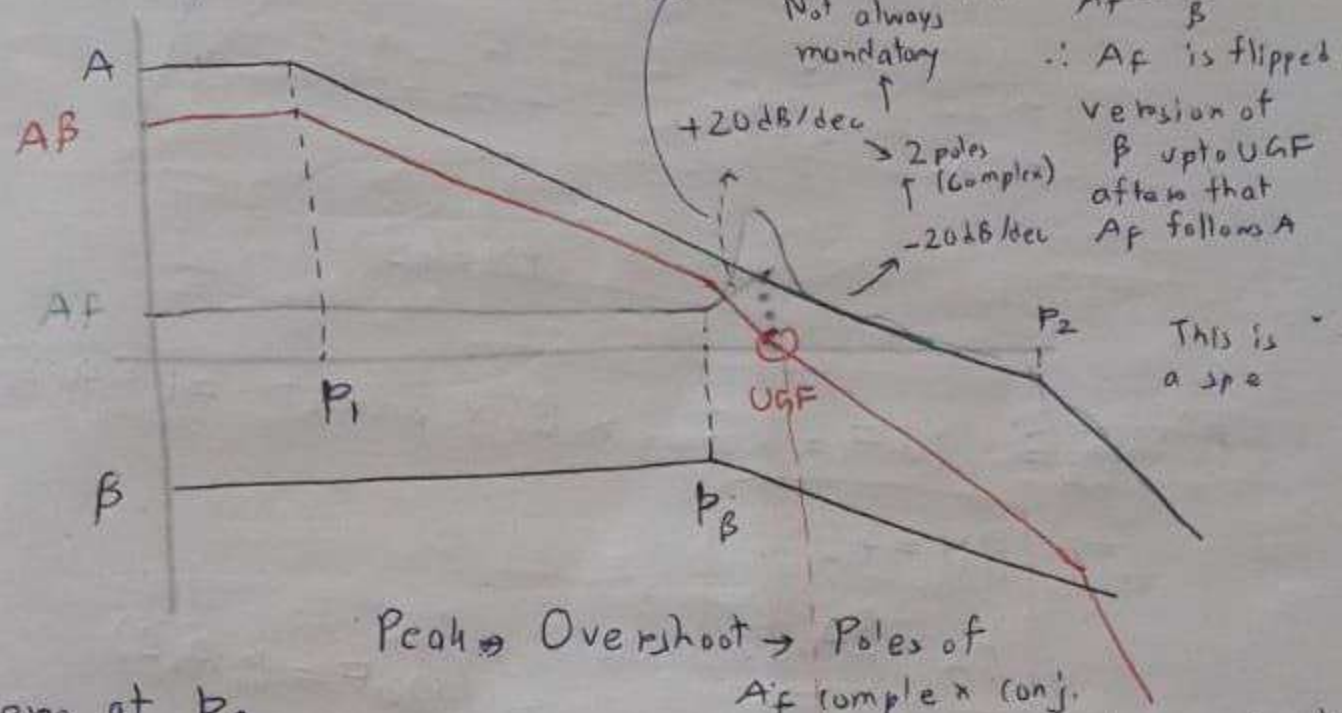
## □ Feedback n/w having a pole.




$$A_f = \frac{A}{1+\beta A}$$

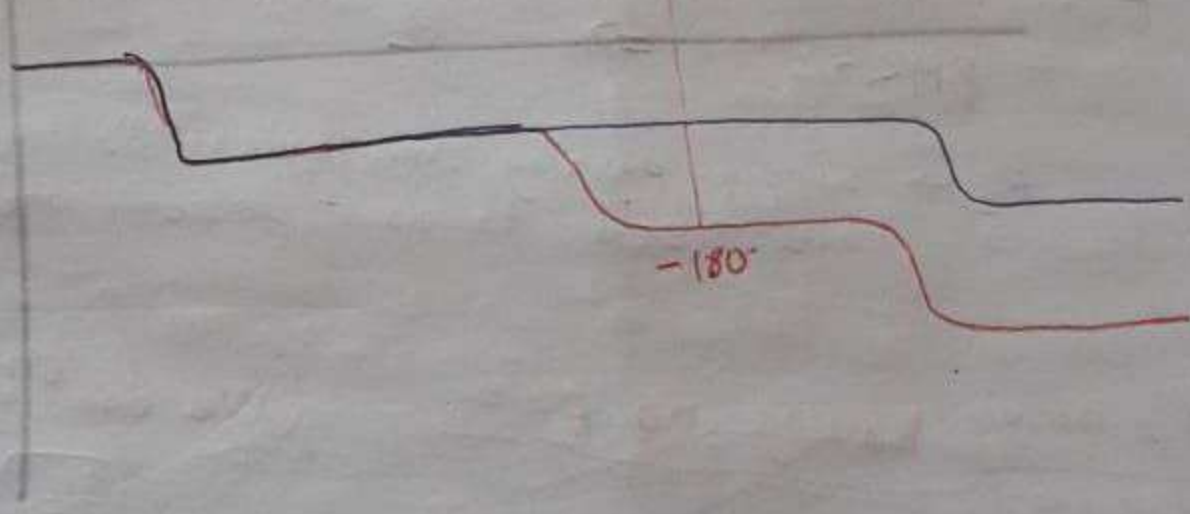
For $\beta A \approx -1$ Close to $-1$ [oscillation tendency] Not always mandatory

$A\beta >> 1$ upto UGF $A_f = \frac{1}{\beta}$ ∴ $A_f$ is flipped version of $\beta$ upto UGF after that $A_f$ follows A




$A_f$ → Zero at $P_\beta$

2 poles ($P_1, P_2$) < UGF → It is expected to have complex conjugate pair



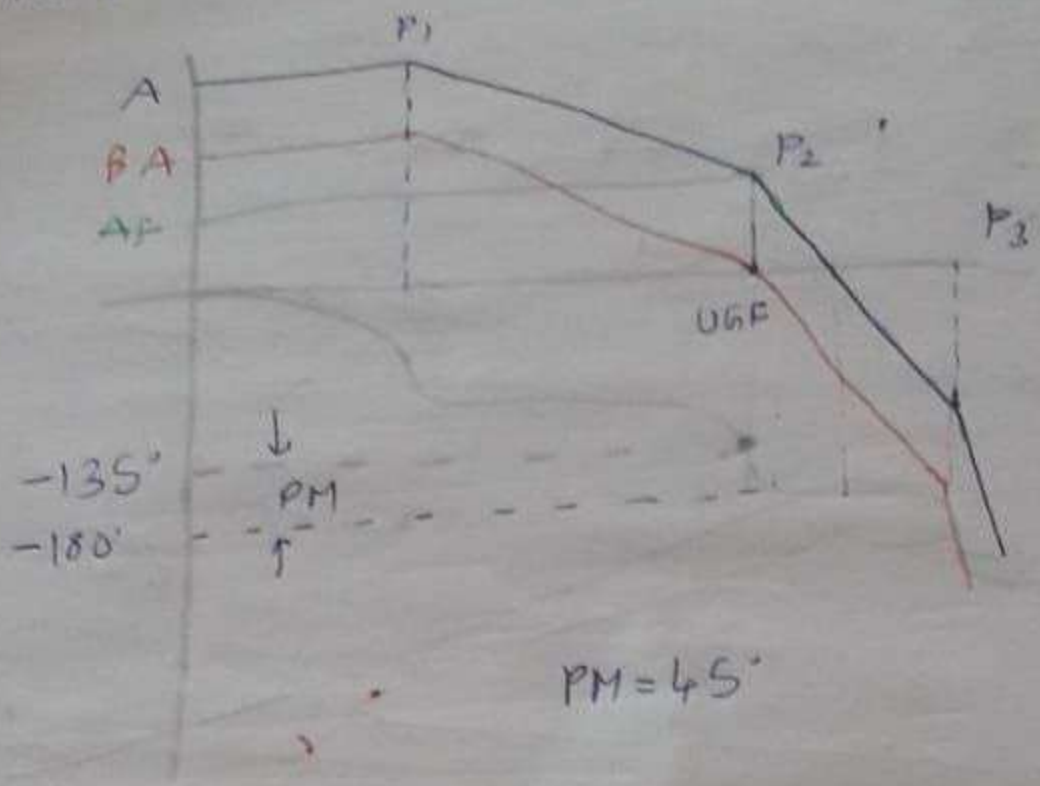

At $\omega$ = UGF, $\angle A\beta = -180°$ → Danger point

Hence don't get happy thinking that $P_1, P_2$ of A are wide apart. [You may have complex conjugates pole after f/b in Closed loop gain].

[Although $P_2 >$ UGF may feel that we are in stable and safe zone but β makes it problematic].

F/b n/w no pole, opamp with 2 poles (effectively)

- For more or less than 45° PM




If $P_2$ = UGF = Gain × B/W product = $(\beta A_0 P_1)$

⇒ **PM = 45°**

**$P_2 = \beta A_0 P_1$**

For PM > 45°, ⇒ $P_2 > (UGF = P_1 A_0 \beta)$

PM < 45° ⇒ $P_2 < (UGF = P_1 A_0 \beta)$

$P_2$ → simply pushing can tradeoff $A_0$.
we need to do it properly and carefully

## F/b n/w having no pole (We don't know β)

D Stability of op-amp eff. with 2 poles

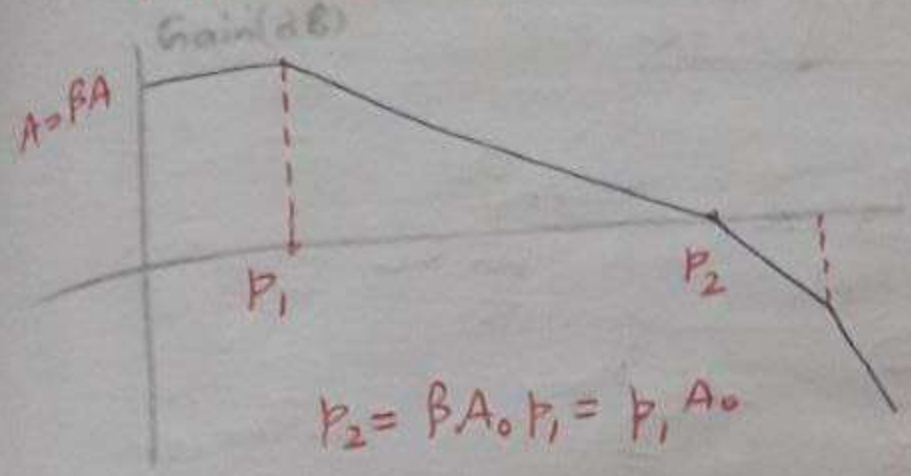
1) > 45° PM
2) > 60° PM

**β = 1** → Worst case scenario

↓

Not worst case scenario for β with pole & UGF,
↳ Even worse

PM = 45°



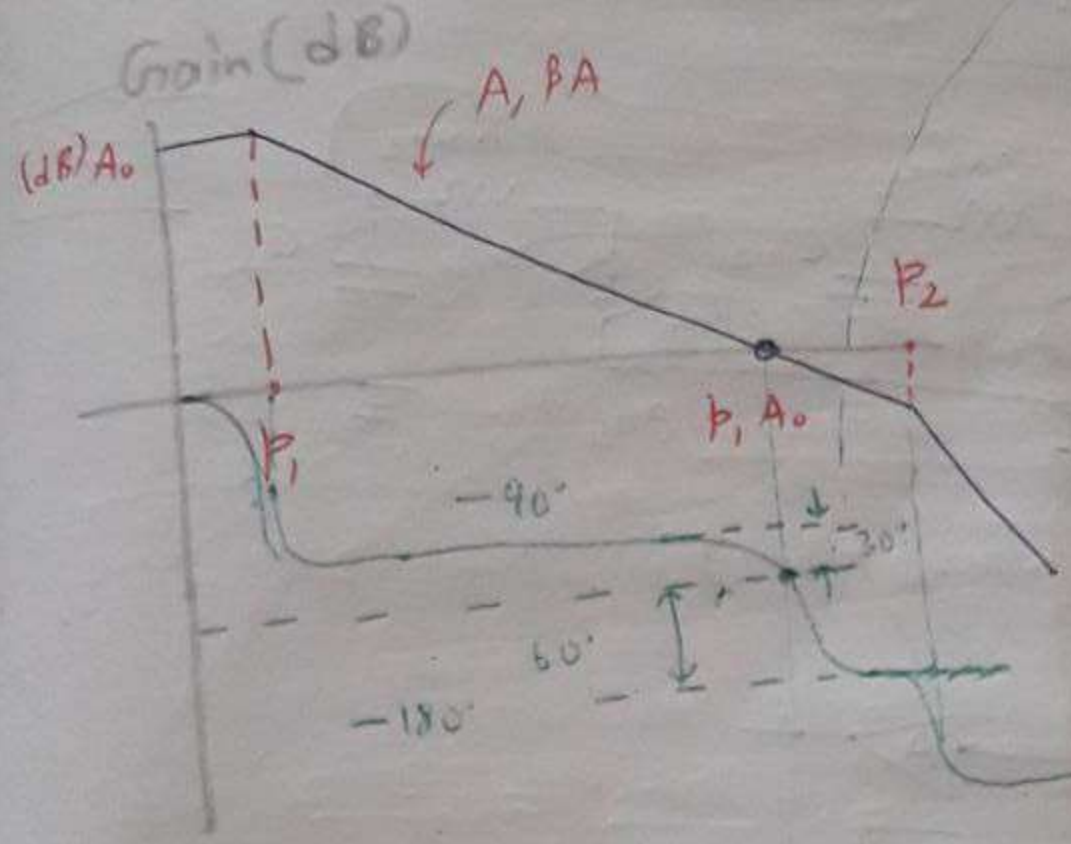

$P_2 = \beta A_0 P_1 = P_1 A_0$

UGF and $P_2$ coincide

UGF $\angle = -120°$

$P_1 \rightarrow -90°$

$P_2 \rightarrow -30°$




Somehow we pushed apart $P_1, P_2$

$$A = \frac{A_0}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)}$$

$$1 + \frac{j\omega}{P_2}$$

$$1 + j\left(\frac{UGF}{P_2}\right) \rightarrow \angle = \tan^{-1}\left(\frac{UGF}{P_2}\right)$$

$$\tan^{-1}\left(\frac{UGF}{P_2}\right) = 30°$$

at UGF $\angle$ due to $P_2 = -30°$

$$\tan^{-1}\left(\frac{UGF}{P_2}\right) = 30° \Rightarrow P_2 = \frac{UGF}{\tan 30°}$$

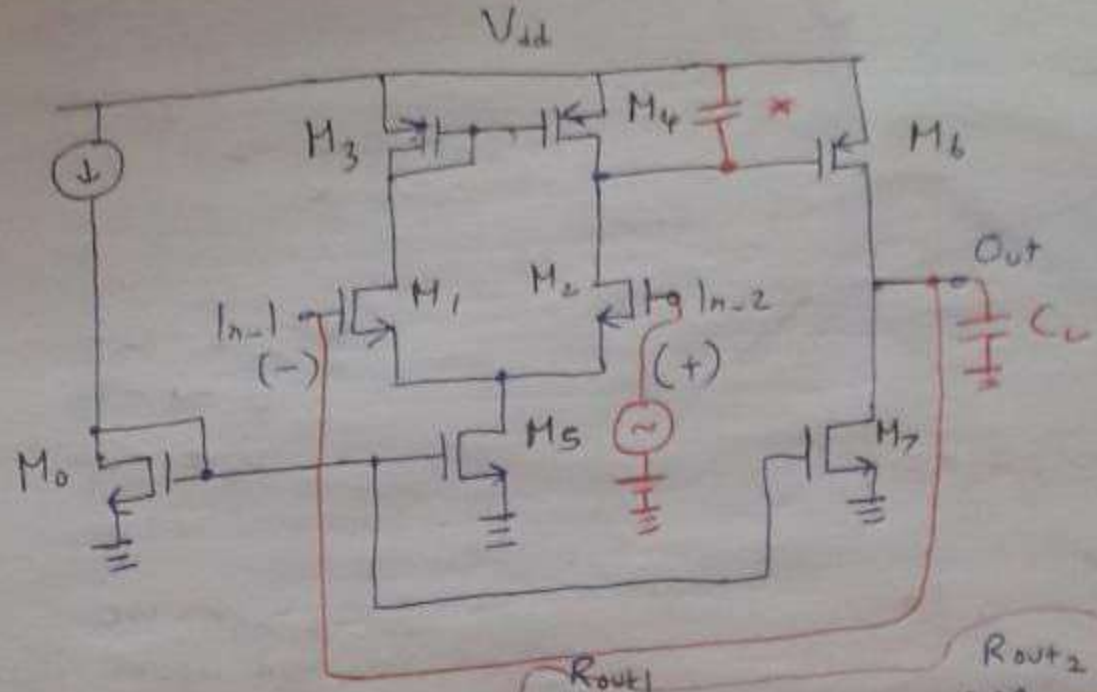
$P_1 A_0 \beta$

General formula

$$P_2 = \frac{UGF}{\tan(90° - PM)}$$

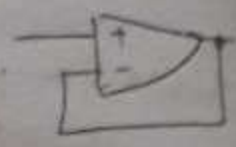
## Stability issue of 2 stage diff. amp (in fb config.)

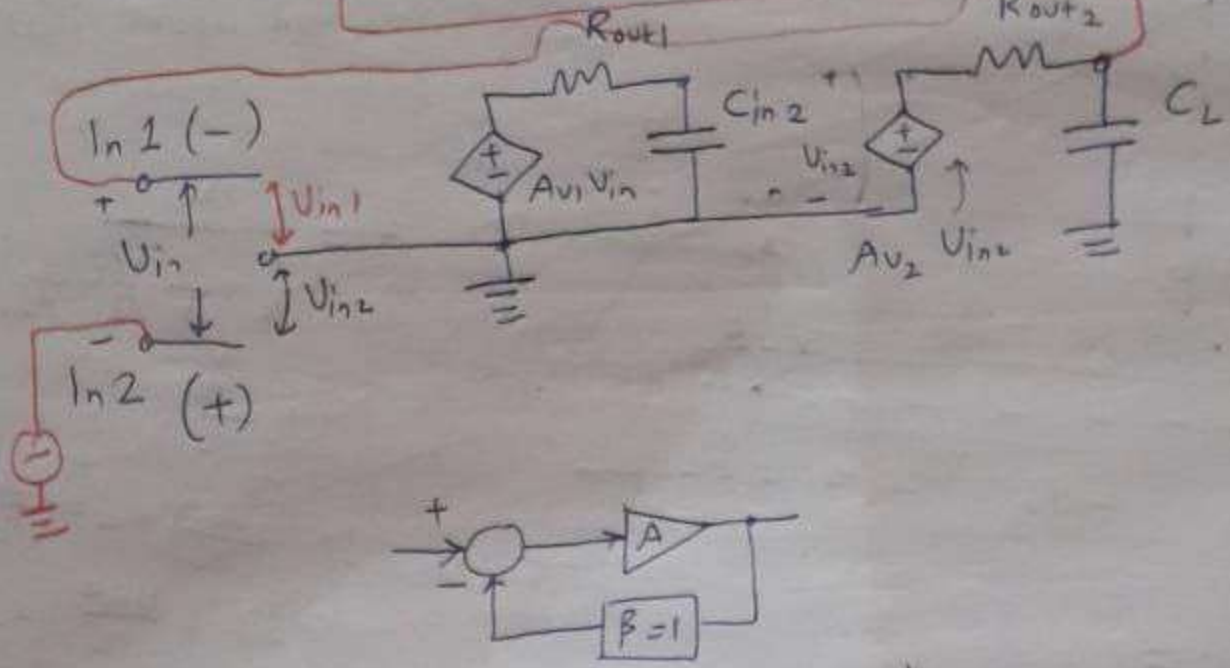
P.T.O.




(-), (+) → wrt Out (2nd stage)

Buffer config









$$p_1 = \frac{1}{R_{out1} C_{in2}}$$

$$p_2 = \frac{1}{R_{out2} C_L}$$

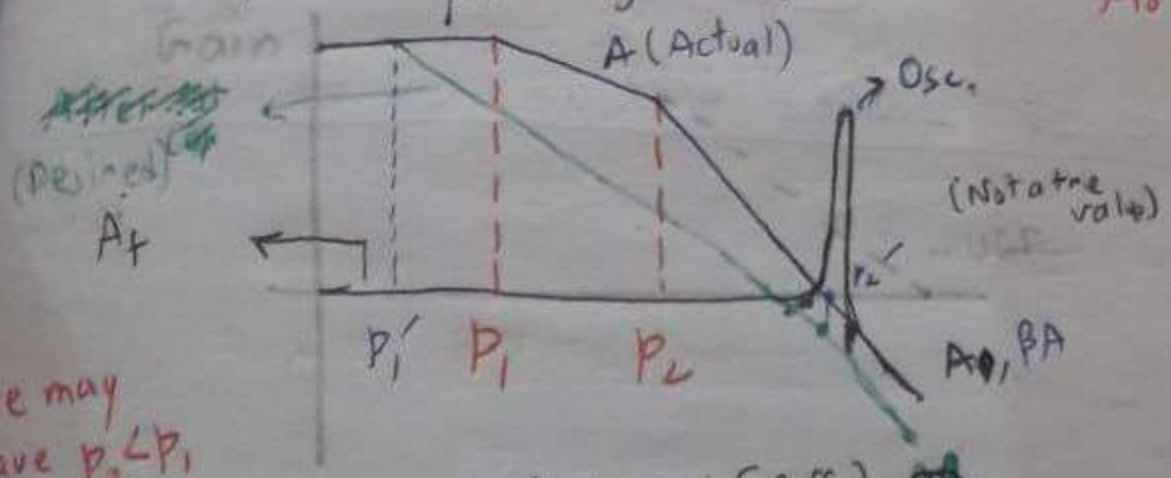
$R_{out1} = r_{o4} \| r_{o2}$

$R_{out2} = r_{o6} \| r_{o7}$

$p_1$, $p_2$ are of same order [Close to each other]

Not good design (Poor PM)

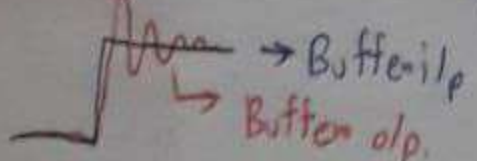
$A_0 = g_{m1} g_{m6} R_{out1} R_{out2}$




PM is poor ∵ $p_2 \ll$ UGF

$p_1$, $p_2$ close → may lead to oscillatory beh. [close to (-1, 0)] Ly Nyquist

We may have $p_2 < p_1$




($\beta = 1$) $A_f \approx 1$ [Buffer] before UGF

2nd stage)

We have to make $P_1$, $P_2$ far apart by pole compensation [like green]

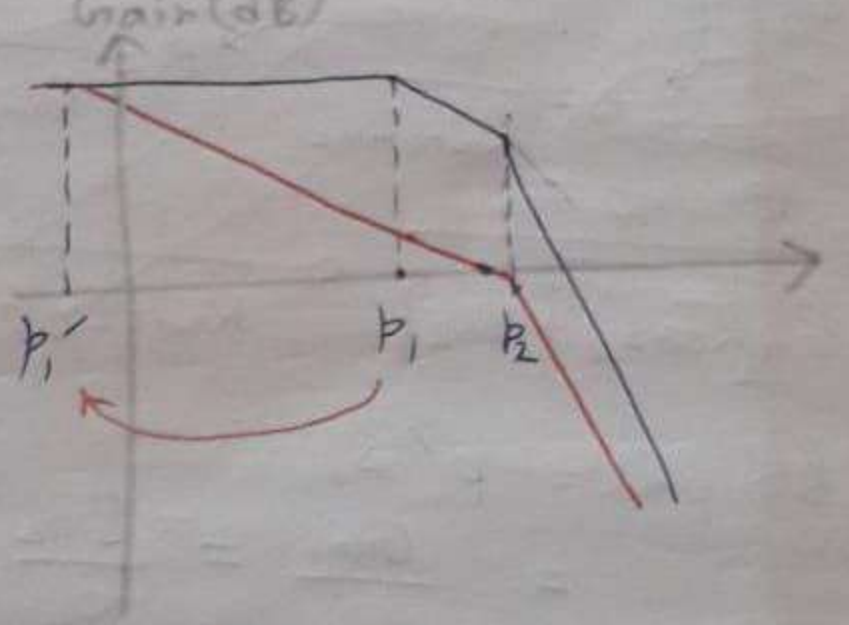
But beyond some point we cannot move $P_2$ away (*) In that case we make $P_1$ smaller by putting a fat cap. shown by (*). [Attempt - Not technique] This has some disadvantages.

(*) 3rd pole can show adversities

Priority: 1) Push $P_2$ far apart
2) Make $P_1$ a bit lower → For 60° PM. (1) Critically damped (2) Good B/w

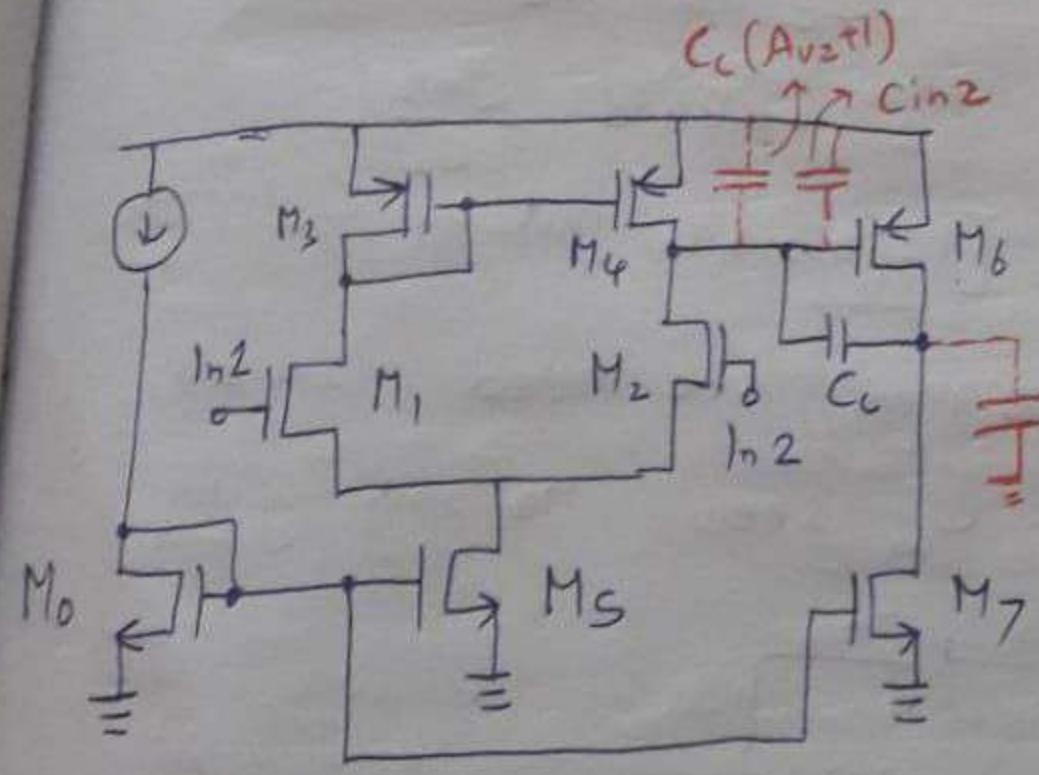
# Pole-Zero Compensation of 2-stage diff. amp.

□ Uses Millen affected capaciton for stability




Putting a fat capacitor as said earlier is really uneffective [Longe space].

So use Miller Effect.

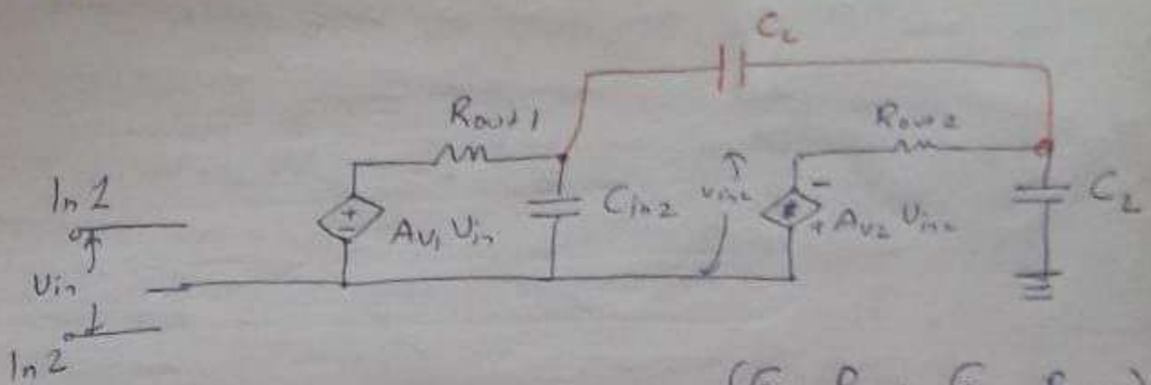



$$A_{v2} = g_{m6}(r_{o6} \| r_{o7})$$

$$C_c\left(1+\frac{1}{A_{v2}}\right)+C_L$$

Major effect on $P_1'$
Very minor effect on $P_2'$ (negligible)

$C_c$ → affected by Miller effect




$(G_{m1} R_{out1} G_{m2} R_{out2})$

$$\text{earlier } A = \frac{A_0}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$

$$p_1 = \frac{1}{R_{out1} C_{in2}} \qquad p_2 = \frac{1}{R_{out2} C_L}$$

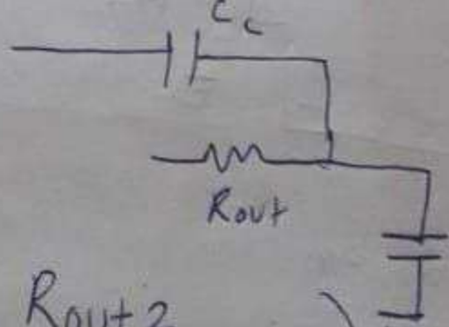
$$p_1' = \frac{1}{R_{out1}\left[C_c(1+G_{m_2} R_{out2}) + C_{in2}\right]} \approx \frac{1}{R_{out1} C_c G_{m_2} R_{out2}}$$

$$UGF = \text{Gain B/W prod.} = p_1' A_0 = \frac{G_{m1}}{C_c} = \frac{g_{m2}}{C_c} \quad (g_m \text{ of } M_2)$$

We need to push $p_2$ beyond $\frac{g_{m2}}{C_c}$.

[Impossible just by $C_c$ miller]

To apply Miller's theorem, we need low o/p impedance. Moreover $C_c$ sees not only gain but also a pole.



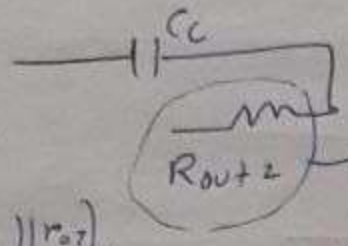

$$\therefore A_{V2} = \left(\frac{G_{m_2} R_{out2}}{1 + s R_{out2}(C_L + C_c)}\right)$$

↓

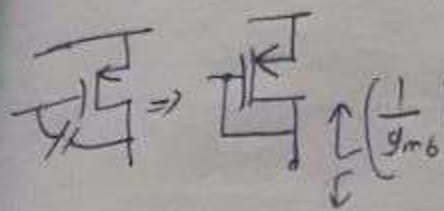
This makes situation complicated

Simplified explanation:

At HF, $C_C \rightarrow$ short and $M_6$ becomes diode connected

$\therefore$ 

$\rightarrow \left(r_{o7} \| \frac{1}{g_{m6}}\right) \rightarrow$ Suddenly small




Now $p_2 = \frac{1}{R_{out2} C_L} \uparrow$ [$\because R_{out2} \downarrow$]

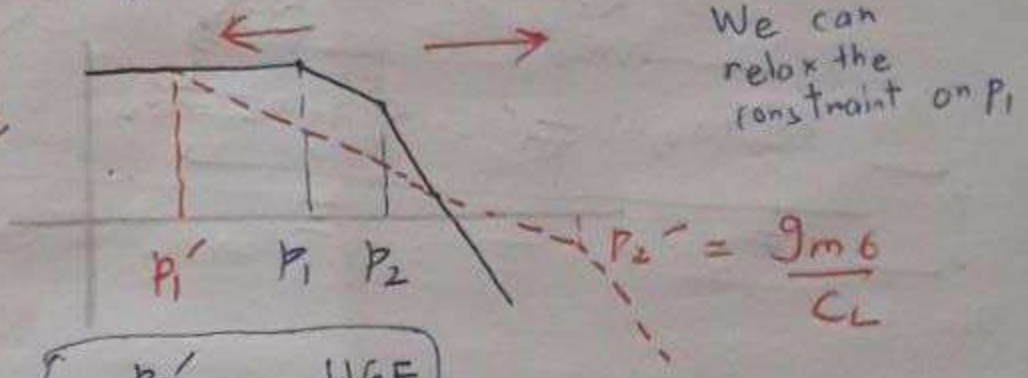
Thus we have shifted the pole $p_2$.

$R_{out2} = \frac{1}{g_{m6}}$ $\qquad p_2' = \frac{g_{m6}}{C_L}$ $\rightarrow$ Pushed to HF

↳ We need not put $p_1$ too low.

Hence Miller's theory should not be applied blindly

This technique is also called Pole-Splitting Technique



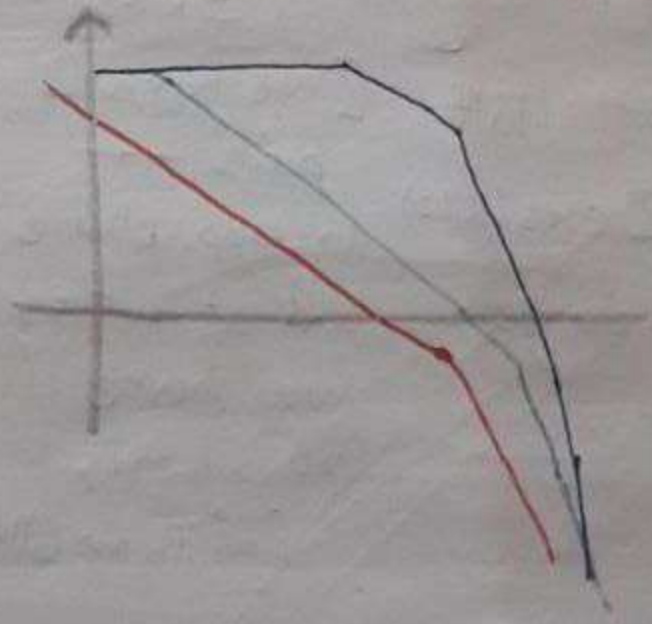

$\frac{p_2'}{\frac{g_{m6}}{C_L}} > \frac{UGF}{\frac{g_{m1}}{C_C}}$ [PM > 45°]

↳ UGF

[Allen-Holberg]

[Watch this part video] → Do it

Lost track




$p_1' = \frac{1}{R_{out1} C_C g_{m2} R_{out2}}$

$p_2' = \frac{g_{m2}}{C_L}$

$Z = \frac{g_{m2}}{C_C}$

IGNORE

Replace Thevenin by Norton

See next page.

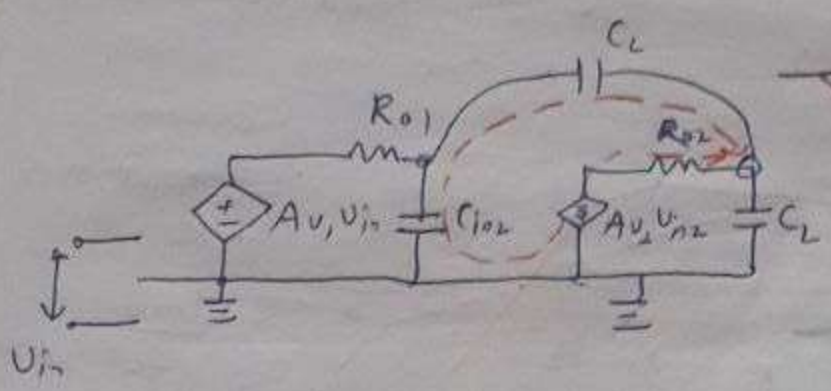
For a given PM

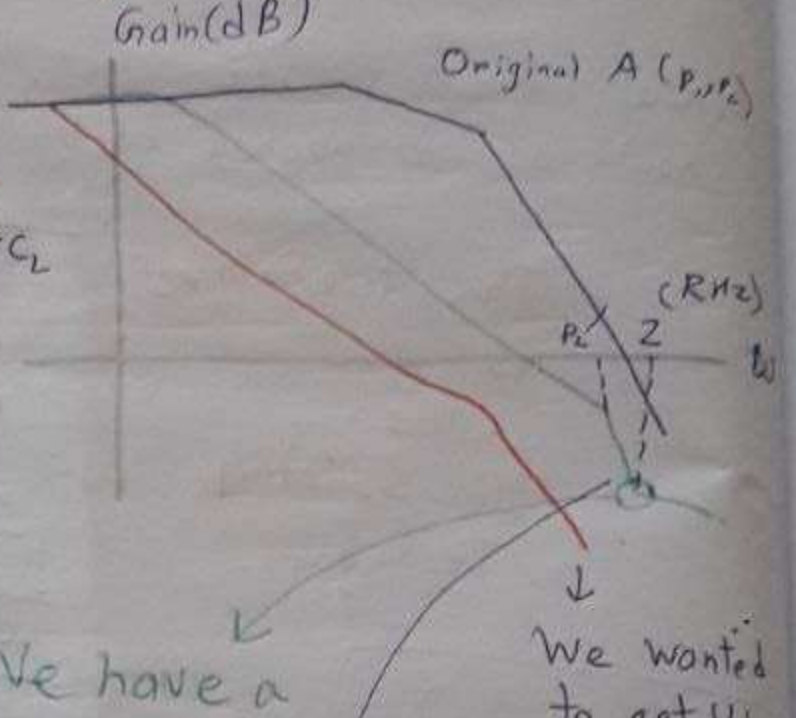
$$P_2' = \frac{UGF}{\tan(90° - PM)}$$

$$\therefore \boxed{\frac{g_{m6}}{C_L} > \frac{g_{m1}}{C_c} \cdot \frac{1}{(\tan(90° - PM))}}$$

## Pole-Zero compensation of 2 stage diff. amp.

□ Use Miller affected Capacitor for Stability.




We have a zero

Right Half Zero (RHz)

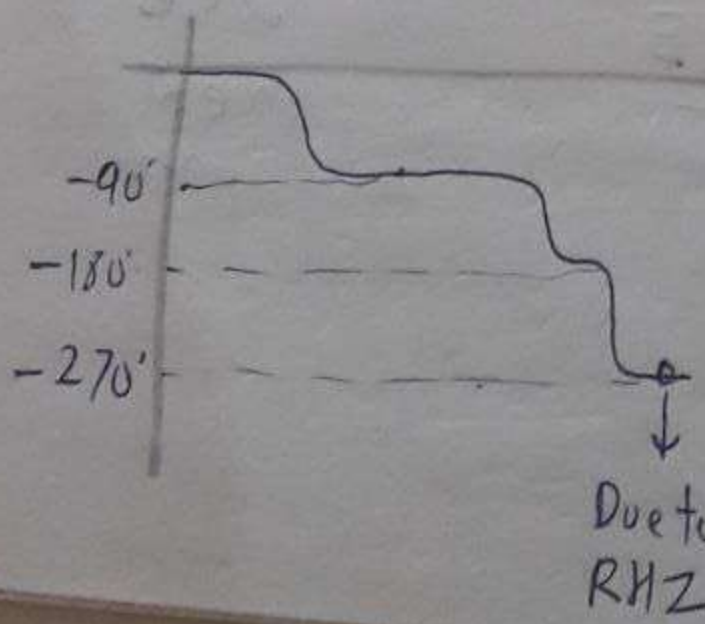
Very dangerous

Further decreases phase towards more −ve

[We have 2 paths — in opp. phase and at a freq. we have no signal, full cancellation)

We wanted to get this But it's not necessary to pull $P_1$ so low

This much pulling of $P_1$ is good enough as 2nd pole is anyways at high freq.



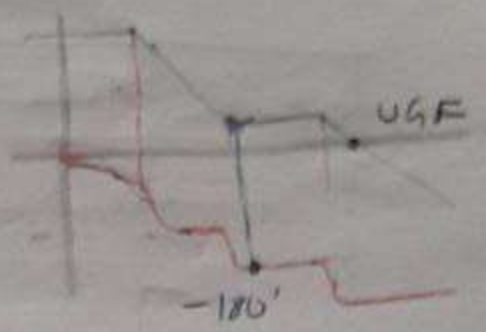
As long as Z is beyond $P_2'$, it is not much of a problem (but eats away a phase)

$Z = \frac{G_{m2}}{C_c}$ $\quad P' = \frac{G_{m2}}{C_L}$ $\quad G_{m_2} \rightarrow g_m$ of 2nd stage.

If Z is b4 $P_2' \rightarrow$ Very dangerous

Even if Z is beyond $P_2'$, it eats away a part of phase

Unstable ←

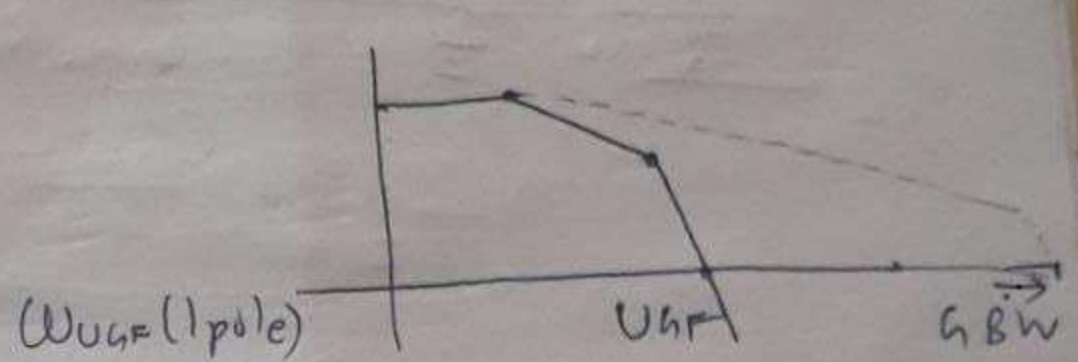



Technique of deriving Z, P'

Replace thevenin voltages by Norton equivalent.

[It is done in next week class]

UGF not always GBW




$\omega_{GBW} = A_0 P_1$ ↑

$\omega_{UGF} = \sqrt{A_0 P_1 P_2}$ [2 pole]

Only for 1 pole

↳ UGF = GBW

$GBW = A_1 P_0$ (always)

For UGF → at HF

$$\frac{A_0}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)} \longrightarrow \frac{A_0}{\frac{s^2}{P_1 P_2}} = 1$$

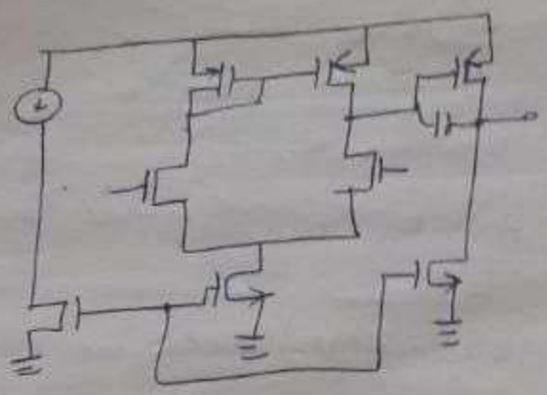
HFreq.

$A_0 P_1 P_2 = \omega^2$

$\omega_{UGF} = \sqrt{A_0 P_1 P_2}$

Week-10 2/11/20

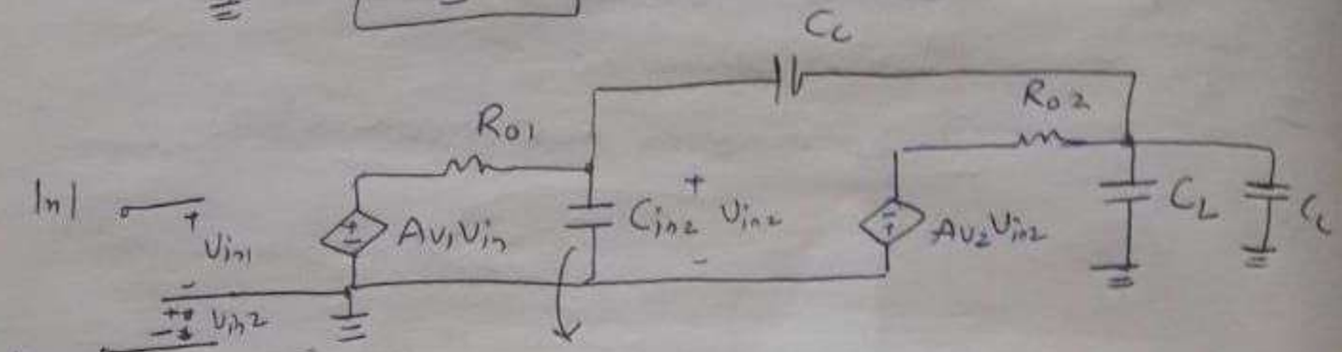
## Pole-Zero Compensation of 2 stage diff. amp.



$$A_{v_1}' = \frac{G_{m_1} R_{o1}}{1 + \frac{s}{P_1}}$$

$$P_1 = \frac{1}{R_{o1}(C_{in2} + C_c)_2}$$

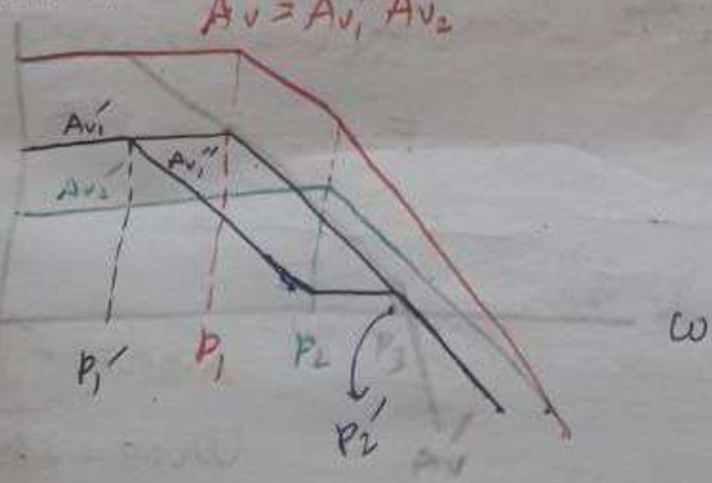
Assuming Miller eff. there




$$C_{in2} + C_c + C_c \frac{G_{m_2} R_{o2}}{(1 + \frac{s}{P_2})}$$

$$P_2 = \frac{1}{R_{o2}(C_L + C_{in2})}$$

Gain(dB)




$$A_{v_2}' = \frac{G_{m_2} R_{o2}}{1 + \frac{s}{P_2}}$$

$$P_2 = \frac{1}{R_{o2}(C_L + C_{in2}')}$$

$P_2$ no effect on $P_1'$. So good. But as we go to higher freq we see effect of $C_c \frac{G_{m_2} R_{o2}}{(1 + \frac{s}{P_2})}$, hence blue curve becomes constant and $A_{v_1}''$ catches up $A_{v_1}'$. So that we get $A_{v_1}'$ (in red) without Miller (top of page)

Including Miller eff. $P_1$ becomes $P_1'$

$$P_1' = \frac{1}{R_{o1}(C_{in2} + C_c + G_{m_2} R_{o2} C_c)}$$

$\downarrow$

$A_{v_1}'$ becomes $A_{v_1}''$

Thus $A_{v_1}''$ has a pole at lower freq $p_1''$ and a zero at $p_2$ and a pole at $p_3$. Green ($A_{v_2}'$) remains unchanged)

Hence the new $A_v = A_{v_1}'' \cdot A_{v_2}'$ becomes as shown by pencil line.

[Pole of $A_{v_2}'$ = Zero of $A_{v_1}'$ = $p_2$]

$p_2' = p_3 \rightarrow$ Defined by $A_{v_1}''$ (can be checked in simulation)

We can say that

$$A_v = \frac{G_{m_1} R_{o1} G_{m_2} R_{o2}}{\left(1+\frac{s}{p_1'}\right)\left(1+\frac{s}{p_2'}\right)}$$

$$p_2' = p_3 = p_2 > \frac{p_1}{p_1'}$$

$\frac{G_{m_2} R_{o2}}{\left(1+\frac{s}{p_2}\right)}$ ⌐ Provides equal shift to $p_2$

We have ignored $C_c$ as a feed forward path, thus we have a new different zero.

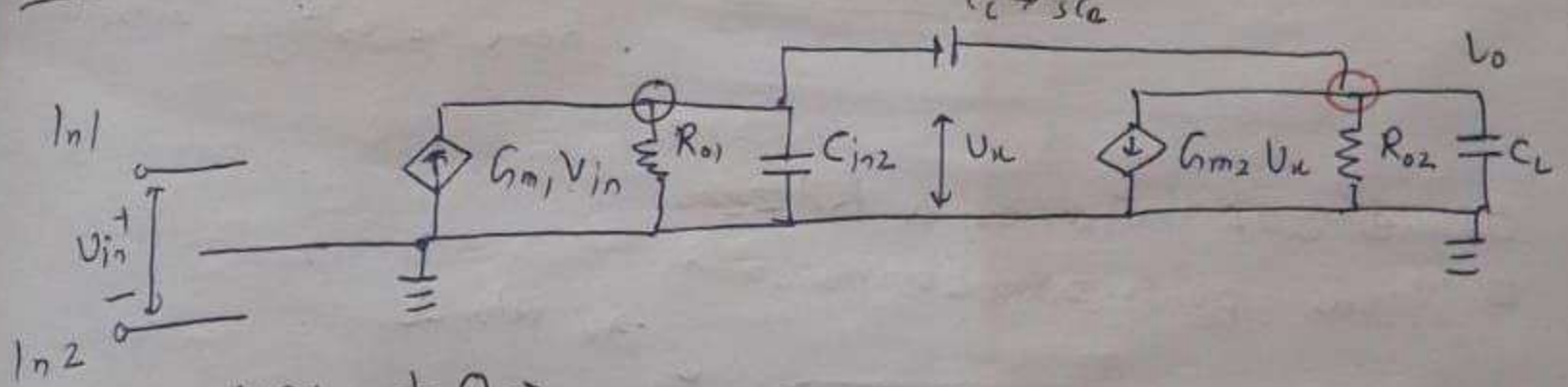
$\frac{p_2}{p_2} = \frac{p_1}{p_1'}$ as for $p_1$ to $p_1'$

$$p_3 = \frac{G_{m_2}}{(C_c + C_L)\left(1+\frac{C_{in2}}{C_c}\right)}$$

Miller Cap: $p_1 \longrightarrow p_1'$

$p_2 \longrightarrow p_3 = p_2'$ (Pole splitting).

## More Accurate Analysis of Miller Compensation Circuit




KCL at O →

$$G_{m_1} V_{in} + sC_c(V_o - V_x) = \frac{V_x}{R_{o1}} + V_x sC_{in2}$$

$$G_{m_1} V_{in} + sC_c V_o = V_x \left\{\frac{1}{R_{o1}} + s(C_c + C_{in2})\right\} \quad -(1)$$

KCL at O →

$$V_x(G_{m_2} - sC_c) = -V_o\left\{\frac{1}{R_{o2}} + s(C_L + C_c)\right\} \quad -(2)$$

$$G_{m_1} R_{o1} R_{o2} (G_{m_2} - sC_c) V_{in}$$
$$= -V_o[(1 + sR_{o2}(C_L + C_c))(1 + sR_{o1}(C_c + C_{in2}))$$
$$+ R_{o1} R_{o2} G_{m_2} sC_c - R_{o1} R_{o2} C_c^2 s^2]$$

$$= -V_o\left[1 + s\{R_{o1}(C_c + C_{in2}) + R_{o2}(C_L + C_c) + R_{o1}R_{o2}G_{m2}C_c\} + s^2\{R_{o1}R_{o2}(C_L C_{in2} + C_c(C_L + C_{in2}))\}\right]$$

$$\frac{V_o}{V_{in}} = -\frac{G_{m1}R_{o1}R_{o2}(G_{m2} - sC_c)}{\{1 + s\underbrace{(R_{o1}R_{o2}G_{m2}C_c + C_{in} + C_L)}_{\downarrow}\}\{1 + \frac{s}{p_2'}\}}$$

1st pole $(p_1')^{-1}$ (dominant term

$$p_2' = \frac{G_{m2}}{C_L + C_{in2} + \frac{C_L C_{in2}}{C_c}} \quad \text{(approx.)} \qquad [R_{o1}R_{o2}G_{m2} \gg R_{o1}, R_{o2}]$$

Apart from $p_1'$, $p_2'$, we have a zero

Numeraton → $G_{m1}R_{o1}R_{o2}(G_{m2} - sC_c)$

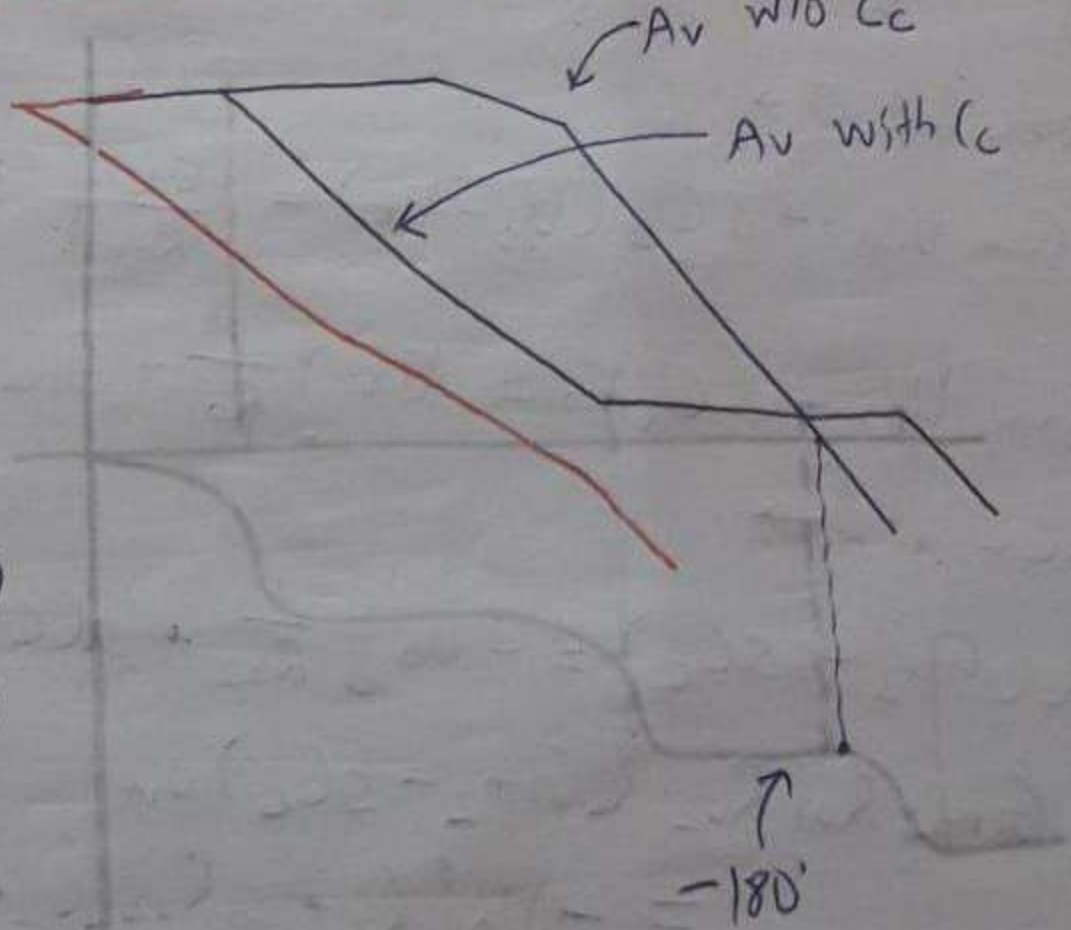
$= G_{m1}G_{m2}R_{o1}R_{o2}\left(1 - \frac{sC_c}{G_{m2}}\right)$

$$Z_{zero} = \frac{G_{m2}}{C_c} \quad (Z_{cc})$$

→ Current through $C_c$ matches $G_{m2}V_x$; hence no voltage across $V_o$.

□ Miller cap introduces a RH zero

□ Needs pole-zero compensation



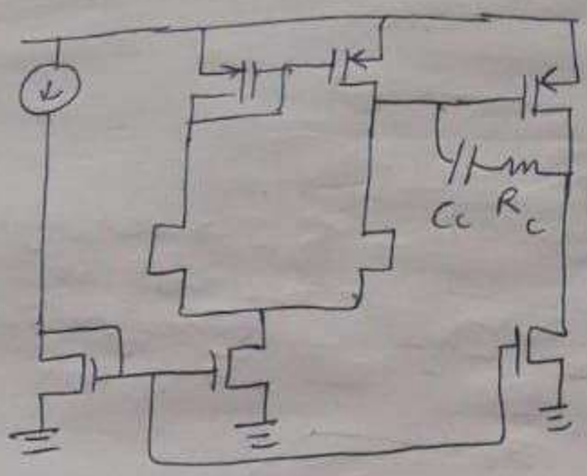

$p_2'$; $Z_c > \frac{p_1' A_{v(low)}}{\tan(90° - PM)}$

Better approach-

Ensure signal through $C_c$ less than $G_{m2} V_x$; we can manage to push the zero to HF.

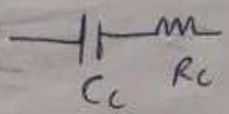
This technique is called pole-zero compensation.

Put series resistor with $C_c$




$$A_{V_2} = \frac{(..)(G_{m2} - sC_c)}{(...)}$$

Some kind of conductance




→ Conductance $= \frac{1}{\frac{1}{sC_c} + R_c}$

$$Z_{CC} = \frac{1}{\left(R_c - \frac{1}{G_{m2}}\right) C_{cc}}$$

$$= \frac{sC_c}{1 + sC_c R_c}$$

$$\therefore \left[ G_{m2} - \frac{sC_c}{1+sC_c R_c} \right]$$

$$= \frac{G_{m2} + s(C_c R_c G_{m2} - C_c)}{(1+sC_c R_c)}$$

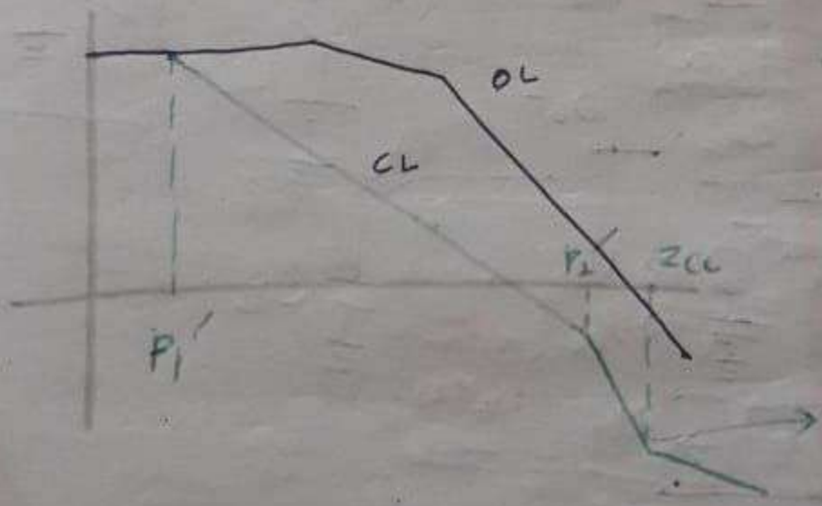
→ zero

← additional pole

To remove zero,

$R_c = \frac{1}{G_{m2}}$ → we push the zero to ∞ freq.

In case $R_c > \frac{1}{G_{m2}}$ → Zero on LHP lane




Matching is imp.

For project consider ↑

$$R_c = \frac{1}{G_{m2}}$$

$Z_{CC} \to \infty$

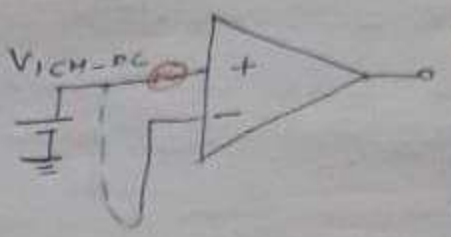
We have a 2 pole system finally.

$$\therefore P_2' > \frac{A_V(0)\, P_1'}{\tan(90° - PM)}$$

Process variation will not create issue

# How to observe performance of an op-amp?

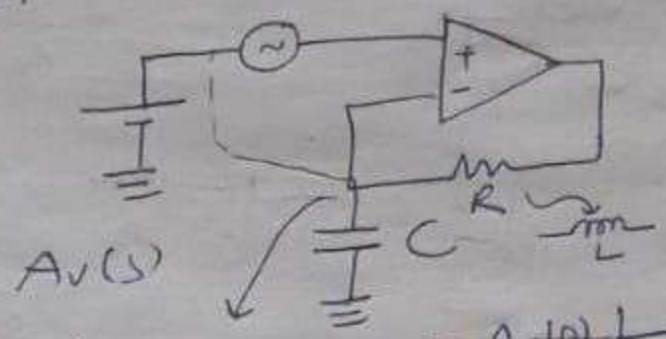
Open loop ] May create issues in transistors in triode



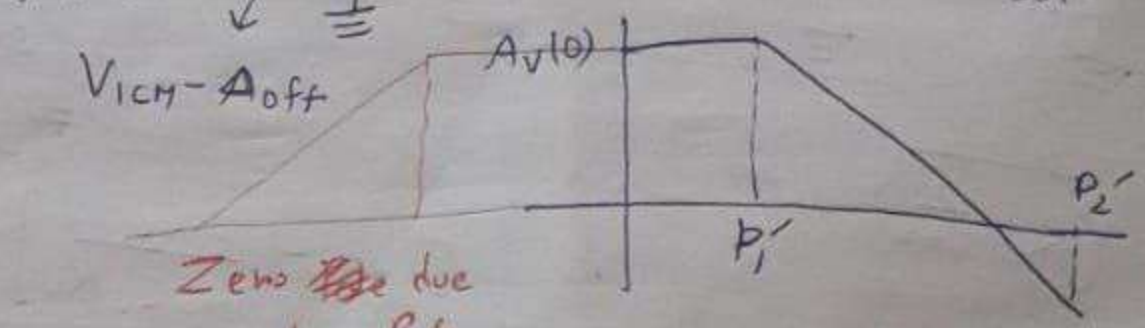

] Problem in this measurement

In case of offset in OPAMP, $M_6$, $M_7$ may go in triode.

Sol.



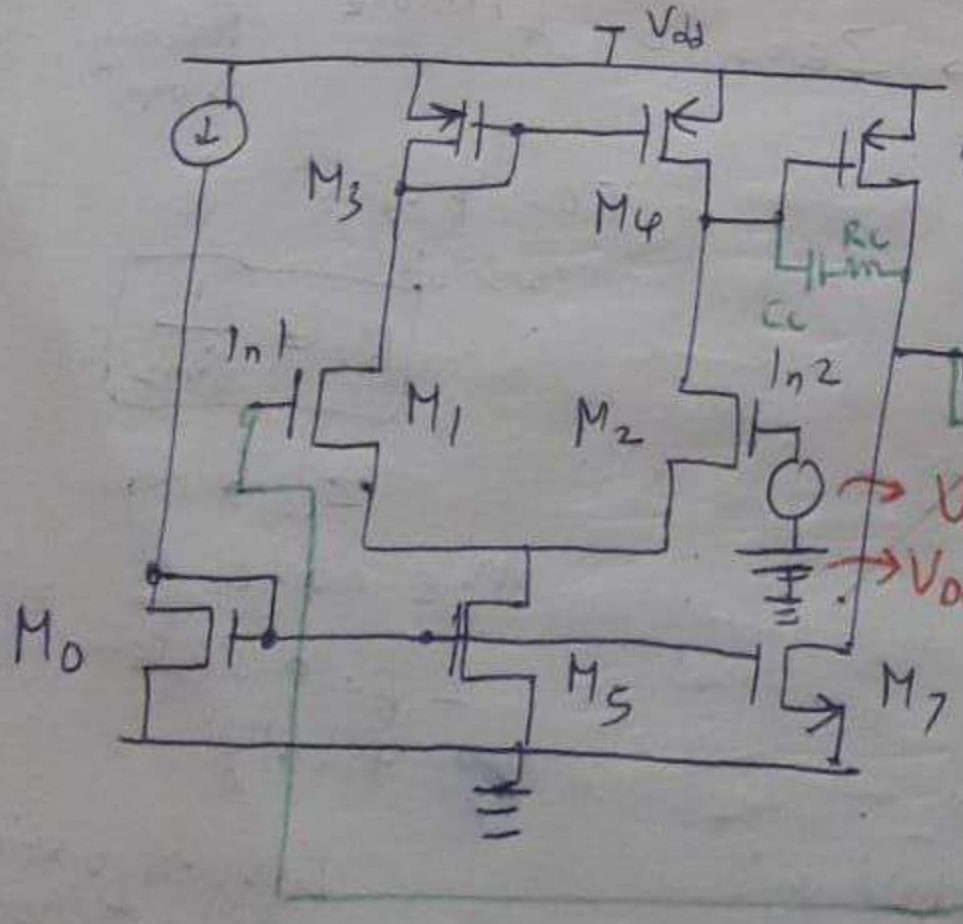

R, C → very high so that no extra signal comes back

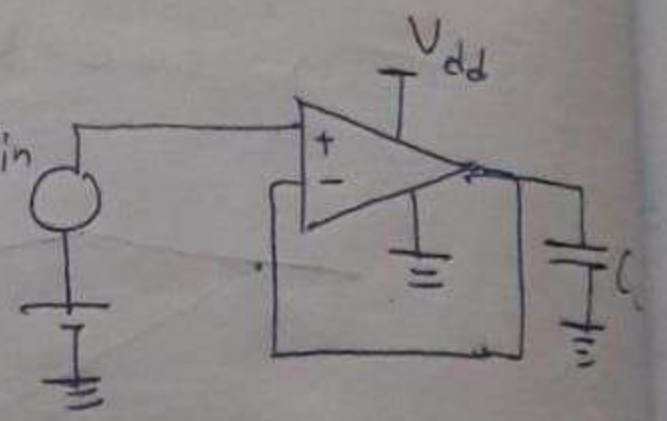


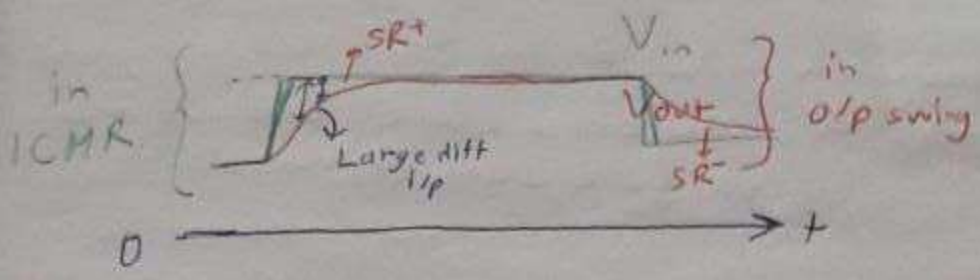

Zero due to RC (Very low freq.)

3/11/20 (Test from 10:30 AM)

# How to observe step response of an OPAMP?






Large diff i/p → $M_2$ strongly on [+ve step]

$M_1$ off

$\Rightarrow I_4 = I_1 = I_5$

$\therefore$ Out of diff stage goes down

(∵ $I_4 - I_5 = 0$ → no current at Rout)

$\Rightarrow V_{SG6} \uparrow$

$\Rightarrow I_6 > I_7$ → Excess current goes into $C_L$ and ramps it up.

The rate at which it goes up is called <u>slew rate</u>.

Settling behaviour

↳ Overshoot, Undershoot

↳ Critical damp., Overdamp, Underdamp.

} Defines step response

Rate at which o/p changes

$*\ SR^+ = \left(\text{+ve step}\right) \dfrac{dV_{out}}{dt} = \dfrac{I_{C_L}}{C_L} = \dfrac{I_{DS5}}{C_C}$ (surprising)

↓ 1st stage determines $SR^+$

$*\ SR^- = \left(\text{-ve step}\right) \dfrac{I_{C_L}}{C_L} = \left\{ \dfrac{I_{DS5}}{C_C},\ \dfrac{I_{DS7}}{(C_L + C_C)} \right\}_{min}$ ↳ PMOS opp.

↓

$I_6 < I_7$

$I_7$ → Current source noon diff. amp. current source

To reduce settling time, we need to improve circuit speed → reduce $t_{rise}$, $t_{sett.}$

5/11/20

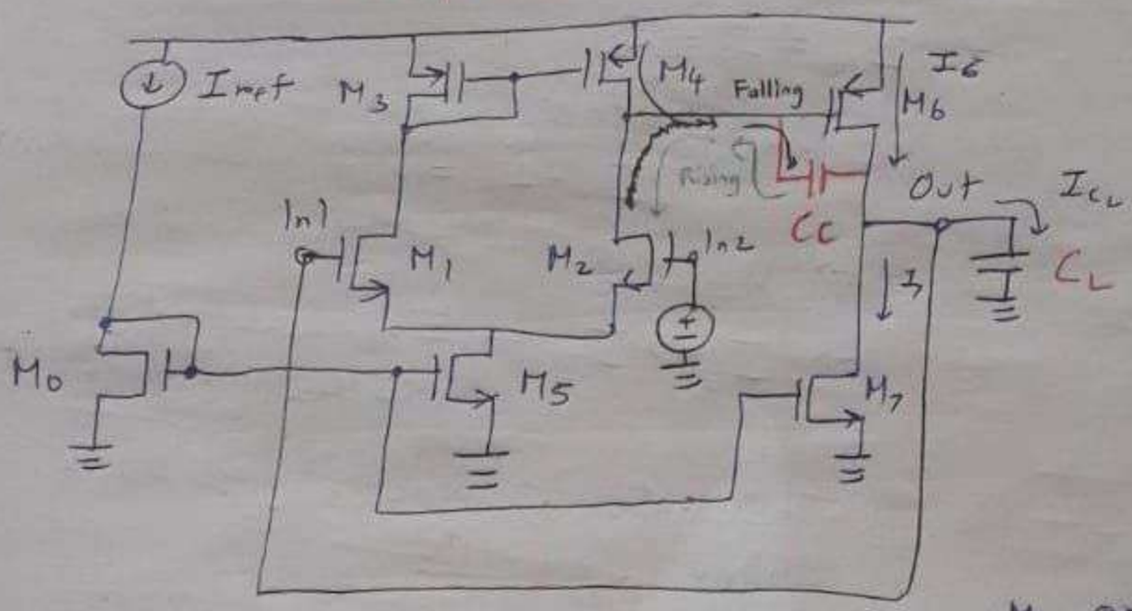
Always check feedback n/w $\beta$ → Sir's Industry experience

Power system → F/b n/w zero cancel bad pole (Good pole zero compensation)

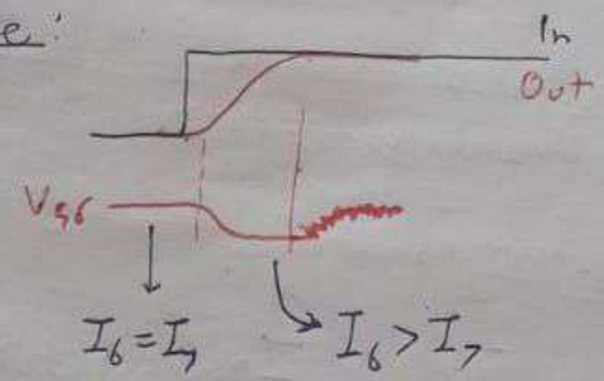
For now let $R_c = 0$

## Slew Rate of Pole-Zero compensated 2 stage diff. amp

– Compensation ckt.




Rising edge:




$M_2$ on (strong)
$M_1$ off

$I_2 = I_5$

Momentarily, $V_{G6}$ is lower so that $I_6 > I_7$

$\Rightarrow I_{CL} = I_6 - I_7 > 0$

$\Rightarrow C_L$ is charged.

$$SR^+ = \frac{dV_o}{dt} = \frac{I_{CL}}{C_L}$$

$C_c$ → Left plate const.
Right plate $V_{out}\uparrow$

$$\frac{dV_{Cc}}{dt} = \frac{dV_o}{dt} \quad [\text{Right plate } V_{out} \text{ changes}] \quad V_o = V_{out}$$

$$\left[\frac{I_{DS5}}{C_c} = \frac{dV_o}{dt} = \frac{I_{CL}}{C_L}\right] \leftarrow \text{41}$$

Although we have $C_{in2}$ and $V_{GS}$ is changing, but

$$\left(\frac{dV_{G6}}{dt}\right) \Big/ \left(\frac{dV_o}{dt}\right) = A_{V2}^{-1} \quad [2\text{nd stage}$$

$\Rightarrow \frac{dV_{G6}}{dt} = \frac{1}{A_{V2}} \frac{dV_o}{dt}$ → Hence we neglect $V_{G6}$ change
$\therefore C_{in2}$ b/w $V_{dd}$, $V_{G6}$ isn't taken into account.

Falling edge

$M_2$ off
$M_1$ (strong on)

$V_{G6} \uparrow$

$\Rightarrow I_6 \downarrow \quad I_6 < I_7$

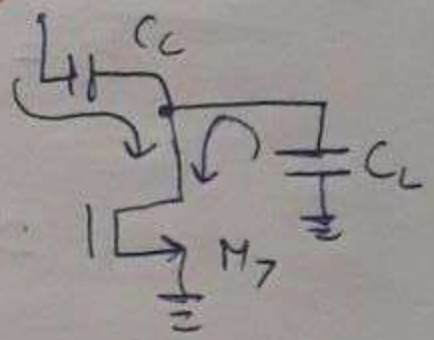
$\Rightarrow I_{CL} < 0$ → Current flows from $C_L$

$$SR^- = \frac{I_{CL}}{C_L} = \frac{I_{DS5}}{C_L}$$

If $V_{G6}$ is high enough to make $M_6$ cutoff,
Stage 2 inactive (Do consider this case in design
↳ Make $I_7$ high to have good SR)
↳ SR depends only on $M_7$.

$$SR^- = \frac{I_{DS7}}{(C_L + C_c)}$$

$M_6$ is off.
$C_L$ discharges through $M_7$
$C_c$ also part of it.




$\therefore$ ** $SR^- = \min\left\{\frac{I_{DS5}}{C_c}, \frac{I_{DS7}}{C_L + C_c}\right\}$

$$SR^+ = \frac{I_{DS5}}{C_c}$$

$$SR^- = \min\left\{\frac{I_{DS5}}{C_c}, \frac{I_{DS7}}{C_L + C_c}\right\}$$

# Numerical

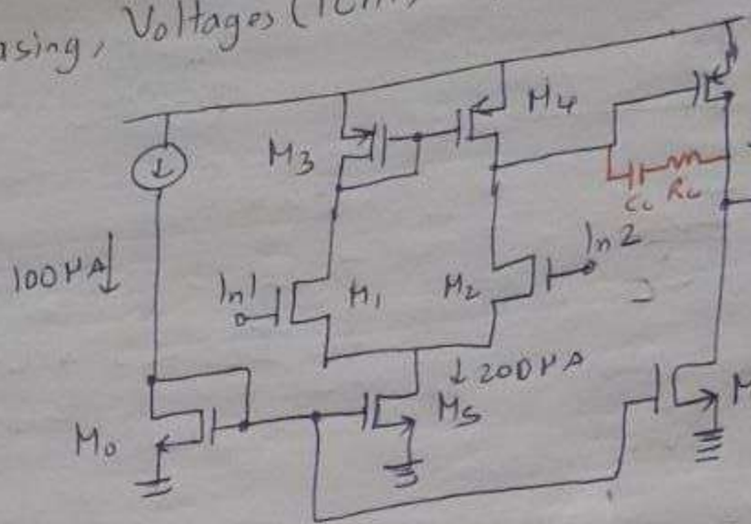
## Sizing of Diff Amp.

Biasing, Voltages (ICMR, OS), $A_d$, $A_c$ → Not discussed much (Done in earlier weeks)

$W_7$: use balance equation

$W_7 = 8 \times 4\mu$

$V_{GS4,6}$, $V_{SG4,6}$




$$A_d = (-G_{m1} R_{o1}) \cdot (-G_{m2} R_{o2})$$

$$A_c = \left(\frac{1}{2 g_{m3} r_{os}} \cdot G_{m2} R_{o2}\right)$$

$$p_1' = \frac{1}{R_{o1}\left(C_{in} + C_c(1 + G_{m2} R_{o2})\right)}$$

$$\simeq \frac{1}{R_{o1} C_c g_{m6} R_{o2}}$$

$$p_2' = \frac{g_{m6}}{(C_L + C_{o_{in2}})}$$

$$Z = \frac{-1}{C_c\left(R_c - \frac{1}{g_{m6}}\right)}$$

$$R_c = \frac{1}{g_{m6}}$$

$$p_3' = \frac{1}{R_c C_c} = \frac{g_{m6}}{C_c}$$

↳ Can be ignored for PM calc.

$$UGF = \frac{g_{m1}}{C_c}, \quad p_2' = \frac{UGF}{\tan(90° - 60°)} \quad [PM = 60°]$$

$$SR^+ = \frac{I_{DS5}}{C_c}$$

$$SR^- = \min\left\{\frac{I_{DS5}}{C_c}, \frac{I_{DS7}}{(C_L + C_c)}\right\}$$

Consider case 2 → $L_6 = 0.25\mu m$
↳ $I_7 \uparrow$ Why changes

[Repeat entire exercise] → By changing $L_6$ we will be able to increase in bandwidth atcost of power and others?

Case 3 → Change $L_3, L_4, L_1, L_2, L_6 = 0.25\mu m$
$L_5, L_7 = 1\mu m$
→ observe changes (gain degradation b/w improvement)

Assignment-8 (Above) → Sunday Midnight

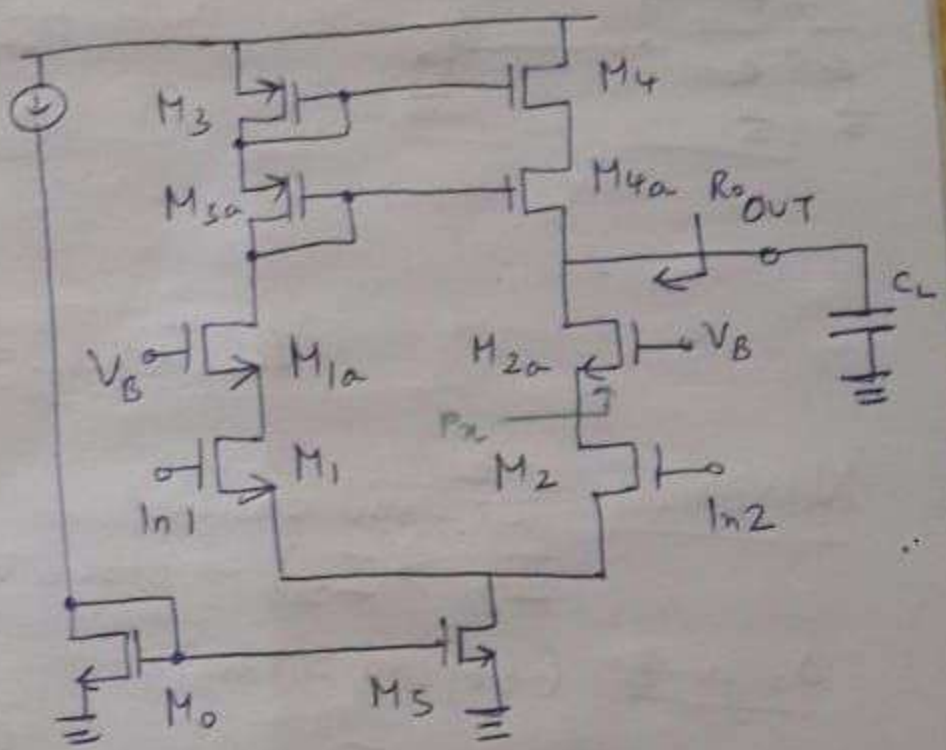
Lower L → Better ICMR

## High Speed Diff. Cascode Amplifier

o/p node is high imp. node
↳ $C_L \gg C_{parasitic}$

$P_1$ → much dominant

$P_1 \ll P_2, P_3$




$$P_1 = \frac{1}{C_L R_{OUT}} \rightarrow \sim g_m r_o^2 \text{ (order)}$$

$$A(0) = g_m R_{OUT}$$

$$GBW = g_{m1} R_{OUT} \times \frac{1}{C_L R_{OUT}} = \frac{g_{m1}}{C_L}$$

$$P_2 > \frac{g_{m1}}{C_L}$$

$$\frac{g_{m2a}}{C_{gs2a}} > \frac{g_{m1}}{C_L}$$

$C_L$ must be large enough
[Can be easily satisfied] ↳ User side spec.

$$\frac{g_{m1}}{2C_{gs2a}} > \frac{g_{m1}}{C_L}$$

What is source of $P_2$?
At HF, $C_L$ shunts OUT
$\therefore r_x = \frac{1}{g_{m2a}}$ $C_x = C_{gs2a}$

$$P_2 = \frac{g_{m2a}}{C_{gs2a}}$$

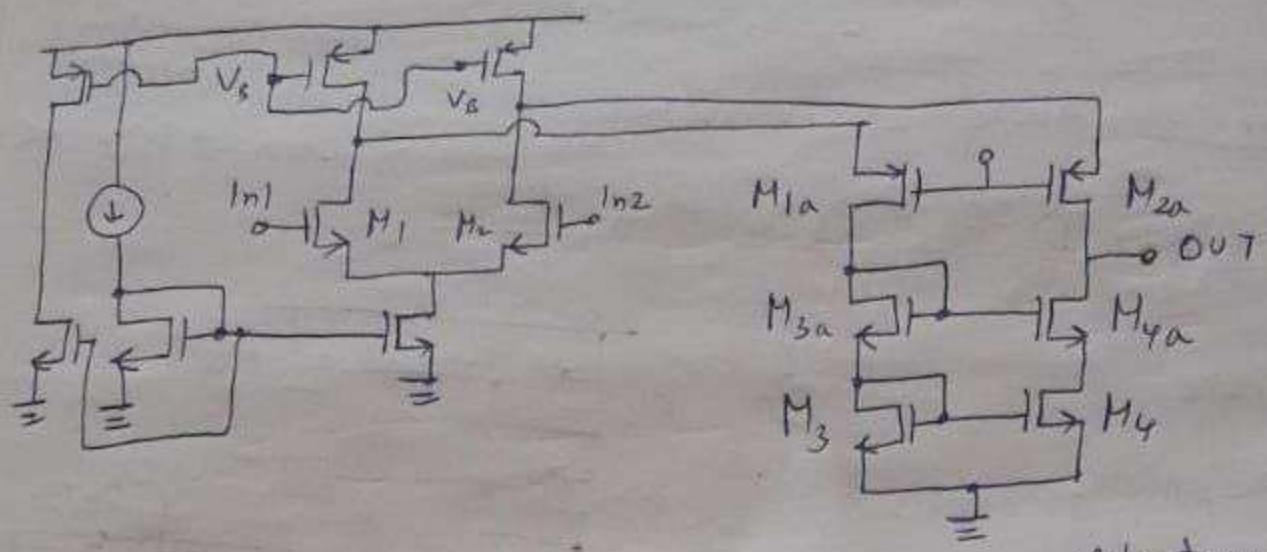
Problem: ICMR and o/p swing don't match
——— $V_{out}$ [Mismatch]

ICMR I

How to use it in buffer config. If they don't match?

## Folded Cascode Amplifier

Above problem is solved




$V_{GS3} + V_{GS3a} = V_Q$

Advantage:
1) Single pole rolloff
↳ Higher BW
2) Better ICMR

Cons:
1) Low OS

Numerical (Folded cascode)

$I_7 > I_5$ → choose value yourself

Assgn-9 (Beyond Sunday) ($W_6 - W_4$ = Yourself)

Find $C_L$ for 60° PM. Choice: $I_7 = 2I_5$

---

For 2 stage opamp:

$G_{m2} = g_{m6}$ $G_{m1} = g_{m2}/g_{m1}$

$$p_1' \cong \frac{1}{R_{o1}(C_C G_{m2} R_{o2})}$$

$$Z \cong -\frac{1}{C_C\left(R_C - \frac{1}{G_{m2}}\right)}$$ (Zero → $R_C = \frac{1}{G_{m2}}$)

$$p_2' \cong \frac{G_{m2}}{C_L + C_{in2}}$$

$$SR^+ = \frac{I_{D5}}{C_C}$$ → NMOS

$$UGF = \frac{G_{m1}}{C_C}$$

$$SR^- = \min\left\{\frac{I_{D5}}{C_C}, \frac{I_{D7}}{C_L + C_C}\right\}$$ → NMOS, PMOS opp.

$$p_2' \cong \frac{UGF}{\tan(90° - PM)}$$

7/11/20

## Numerical (Assignment)

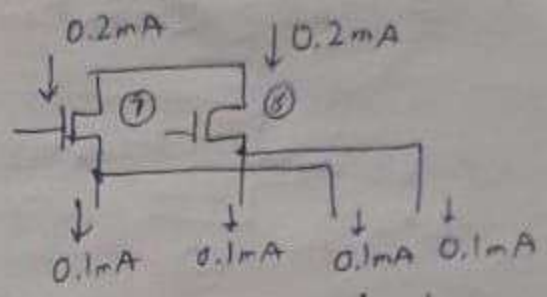
having large signal

$$\frac{I_S}{I_o} = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_0} = \frac{4\times4}{2\times4} = 2$$

$I_S = 2 \times 0.1 = 0.2\,mA$

$I_1 = I_2 = 0.1\,mA$

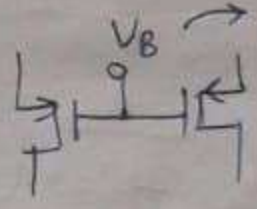
Now instead $I_{D7} = I_{D5}$




For quiescent and common mode
→ $V_{OUT} = V_{D3a}$

Determine $V_{GS3a}, V_{GS3}$

* $V_{OUT} = V_{D3a}$
$= V_{GS3} + V_{GS3a}$




→ defines $V_{out}$ of diff stage

$V_{GS1} - V_{Th1} = 0.25V$

$V_{G1} = 0.3 + 0.25$
$= 0.55V$

$V_{OUT1} = 1.1V$ → Saturation $M_{2a}$ safely
$V_{G1a} = 1.1V$

$V_{SG1a} - |V_{thp}| = 0.25V$

$\Rightarrow V_{SG1a} = 0.35 + 0.25 = 0.6V$

$ICMR^- = V_{GS1} + V_{dsat5} = 0.55 + 0.5 = 1.05V$

$ICMR^+$ $V_{OUT}$ (stage1) $= 1.7V$ → Determined by $M_{1a}$ $V_{SG1a}$

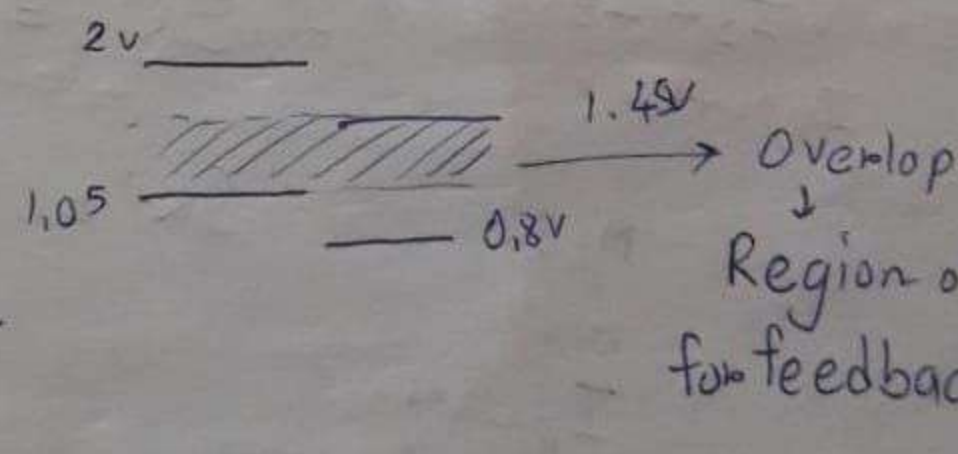
$= V_{OUT} + V_{Tn} = 1.7 + 0.3 = 2V$

OS: $V_{G3} - V_{Tn}$ (min) ; $V_{G2a} + |V_{tp}|$

$1.1 - 0.3$ $\quad$ $1.1 + 0.35$

$= 0.8$ $\quad$ $= 1.45$

ICMR

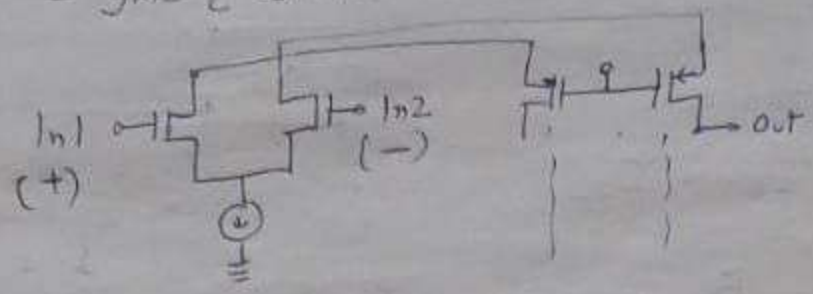


## Small signal, stability

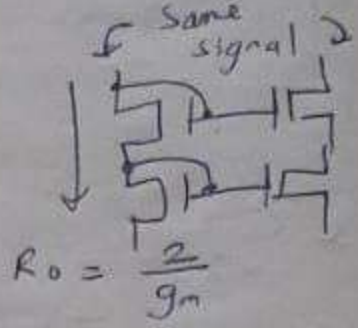
* $A_d = G_{m1} R_{out}$ $\quad (r_{o2} \| r_{o8})$

$= g_{m2} \left( g_{m2a} r_{o2a} \| r_{o4a} \| r_{o4} g_{m4a} \right)$

$= g_{m2} \{ g_{m4a} r_{o4a} r_{o4} \| g_{m2a} r_{o2a} (r_{o2} \| r_{o8}) \}$




* $A_c = \frac{g_{m1}}{1 + g_{m1} 2 r_{os}} \times \left( \frac{1}{g_{m3}} + \frac{1}{g_{m3a}} \right)$




$\simeq \frac{1}{2 r_{os}} \left( \frac{1}{g_{m3}} + \frac{1}{g_{m3a}} \right)$

* $P_1 = \frac{1}{R_{out} C_L}$ $\qquad GBW = \frac{G_{m1}}{C_L}$ $\qquad \left( G_{m1} R_{out} \times \frac{1}{R_{out} C_L} \right)$

$= UGF$

* $P_2 = \frac{g_{m2a}}{C_{gs2a}}$

$P_2 \geq \frac{UGF}{\tan(90^\circ - PM)}$

* $\frac{g_{m2a}}{C_{gs2a}} \geq \frac{g_{m1}}{C_L} \cdot \frac{1}{\tan(90^\circ - PM)}$

* SR

$M_1$ off $M_2$ on $\qquad$ But $I_7$ carries entire current

$I_2 = I_5$

$I_8$ no flow $\qquad \Rightarrow SR^- = \frac{I_{DSS}}{C_L}$ $\qquad$ (Even if $I_7, I_7 > I_5$)

$M_1$ on

$M_2$ off $\qquad SR^+ = \frac{I_{DSS}}{C_L}$

$I_8$ carries entire current

If $I_{DS7} = I_{DS8} > I_{DSS}$, then also SR is defined by $I_{DSS}$

Word of Caution:

$$P_1 = \frac{1}{R_{out} C_L}, \quad GBW = \frac{g_{m1}}{C_L}, \quad P_2 = \frac{g_{m6a}}{C_{gs6a}}$$

$C_L$ should have a min. value for some proper P.M.

$$P_2 > \frac{GBW}{\tan(90° - PM)}$$

Assignment-8

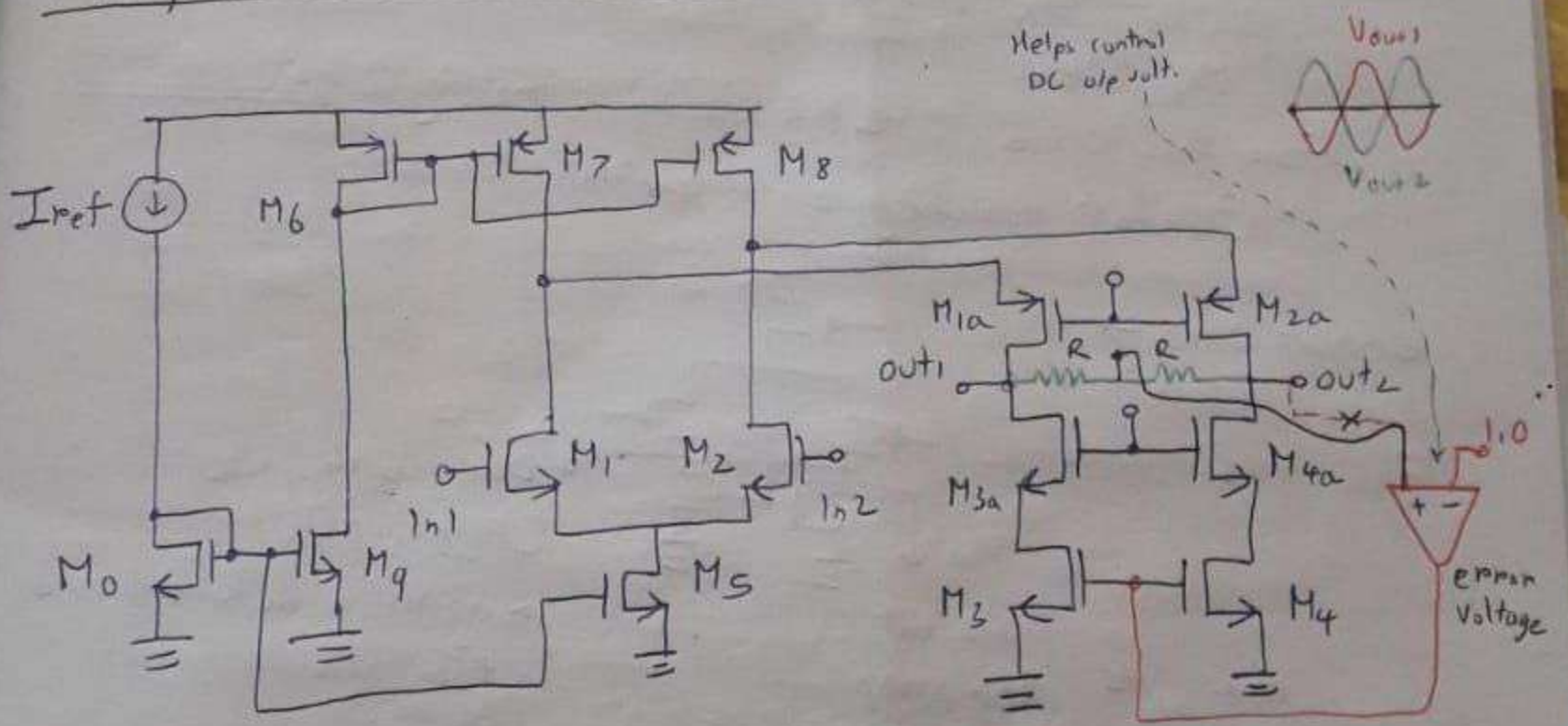
$W_9 = ?$, ICMR, OS, $A_d$, $A_L$

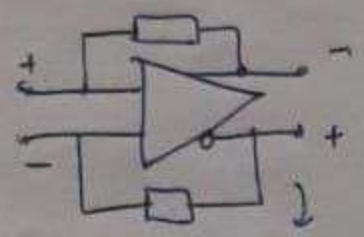
Calculate $C_L$ for PM = 60°, SR and UGF

Take $V_{GS0} = 1.1V$ [But not optimum]

Assgn-7,8 → Monday Midnight Submission

# Fully Differential Folded Cascode Amplifier



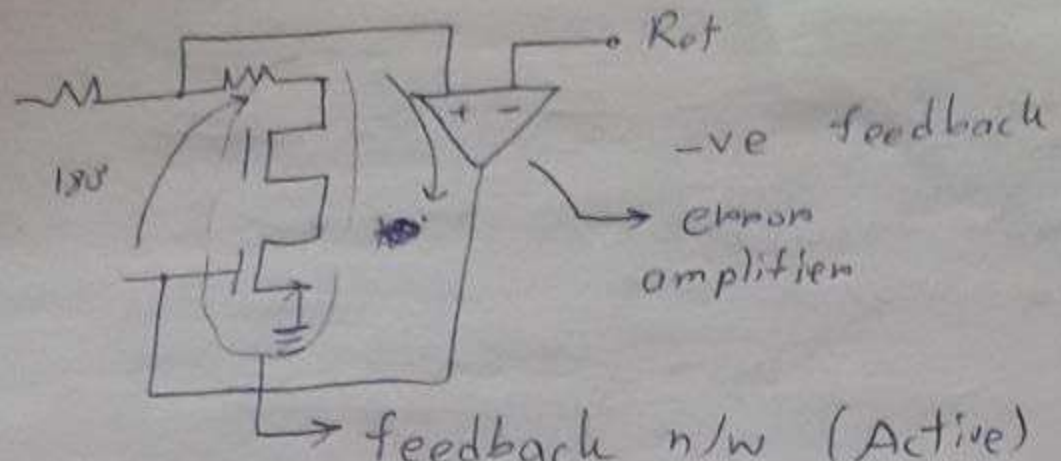
$$\frac{V_{out2} - V_{out1}}{V_{in2} - V_{in1}} = A_d = -g_{m1}(R_{out}) \quad \text{(+ve)}$$

$A_d$ = +ve $\quad \frac{V_{out2} - V_{out1}}{V_{in1} - V_{in2}}$

$$A_d \text{ (single)} = -\frac{g_{m1} R_{out}}{2}$$

Once we release the diode connection at $M_3$, $M_{3a}$; it is difficult to say the DC bias points at $out_1$, $out_2$ because pull down and pull up side both are high impedance.

□ Solution: Common Mode DC Feedback




CS amp. with cascode

Loop gain: $|\beta A| < 1$ (Stability)

We have to ensure sufficient P.M.

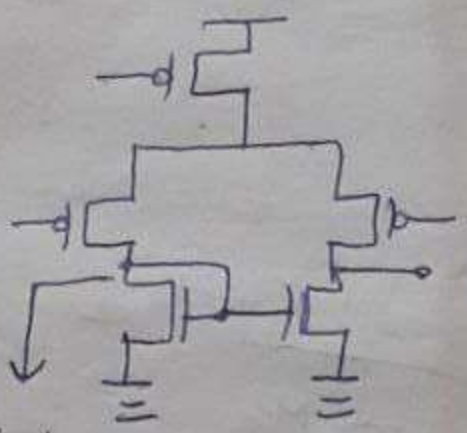
Input DC level of error amplifier should adjust $V_{ref}$, $V_{out}$.

Output level of error amplifier should be compliant with $M_4$, $M_{4a}$.

For this case, ICMR and OS matching is not important.

Current matching is important.

error amp. →



↓ Dont use this pole [High imp.]

→ again a dominant pole in f/b n/w

adv. ← pole but far away (not so high gain - not an issue)

Never implement error amplifier as 2 stage.

→ We will have 3 poles → 1 Pole of f/b n/w

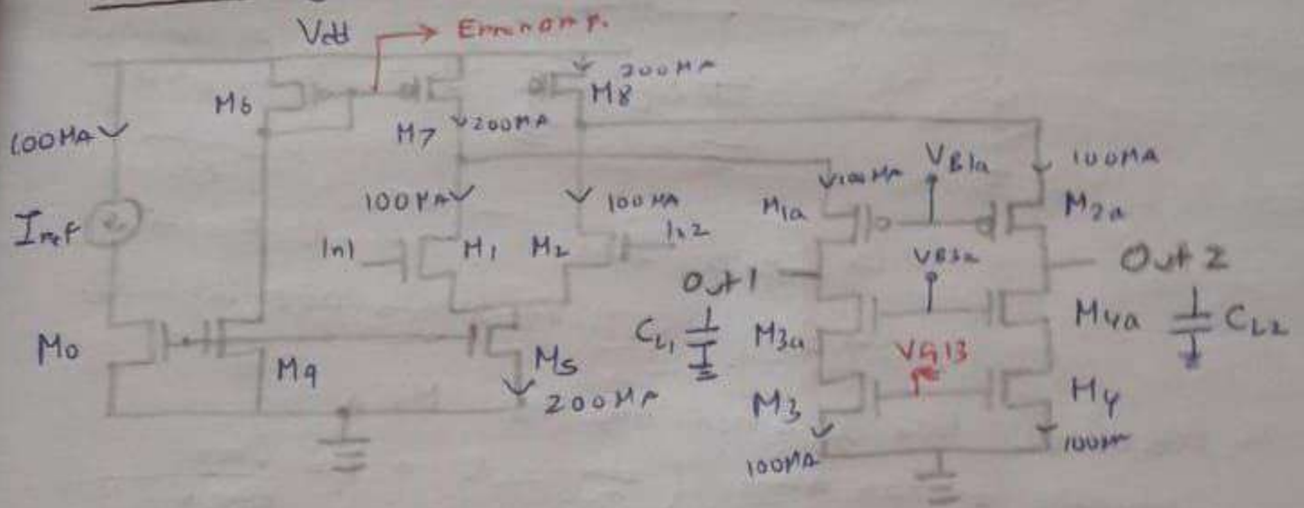
→ 2 poles of err. amp.

Week-11
9/11/20

# Applications of OP-AMP

- ☐ CMFB
- ☐ Voltage to Current converter
- ☐ Linear Regulator
- ☐ Current reference circuit
- ☐ Voltage reference circuit

## CMFB (Numerical)




$I_{SD7} = I_{DS1} + I_{DS3}$

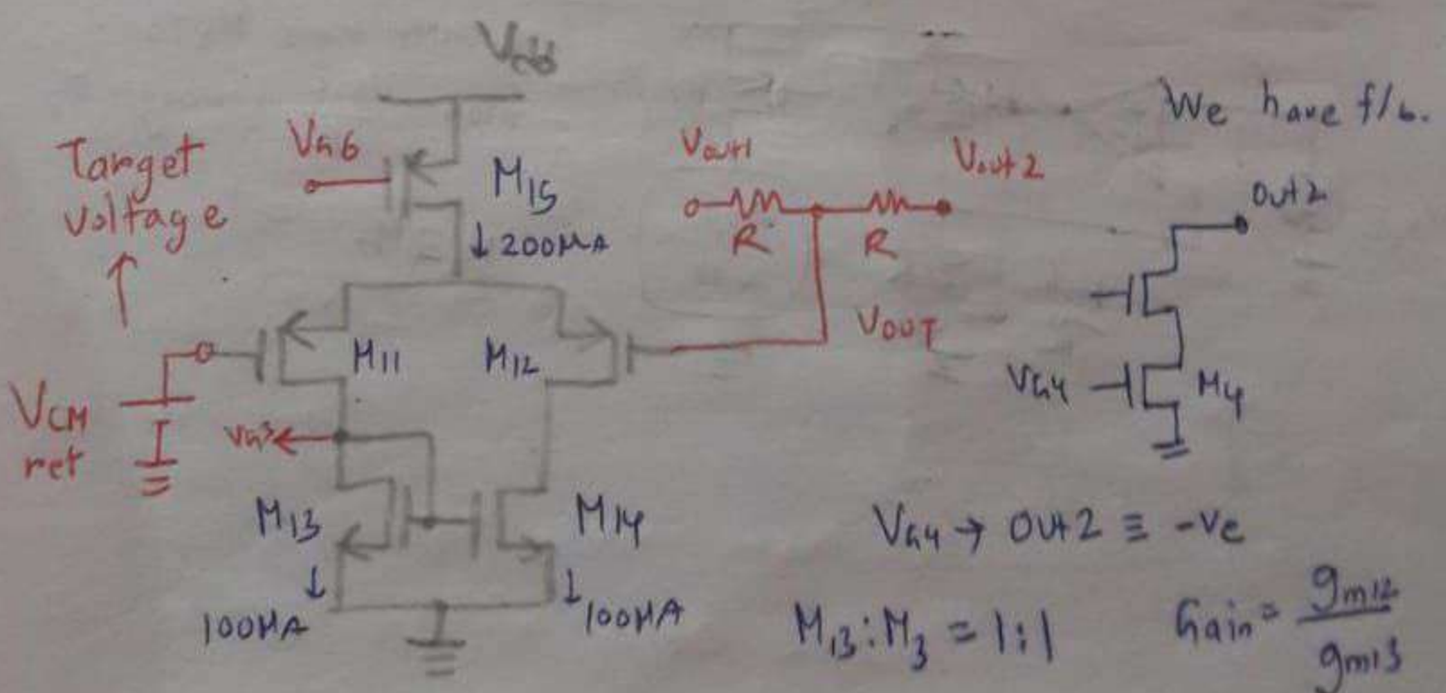
$V_{G3}$ can be tuned to make $I_3 = 100MA$ [1st order balance matching]

2nd order?

↳ Out1 dependenton

$\lambda$s of pullup and pulldown

We need to do something to get rid of 2nd order issues including voltage, temp. deviation → Error amplifier




$V_{G4} \rightarrow OUT2 \equiv -ve$

$M_{13} : M_3 = 1:1$

$Gain = \frac{g_{m14}}{g_{m13}}$

$M_{15}$: $W_{15} = (8 \times 10\mu m = W_7)$ → Same current (200μA)

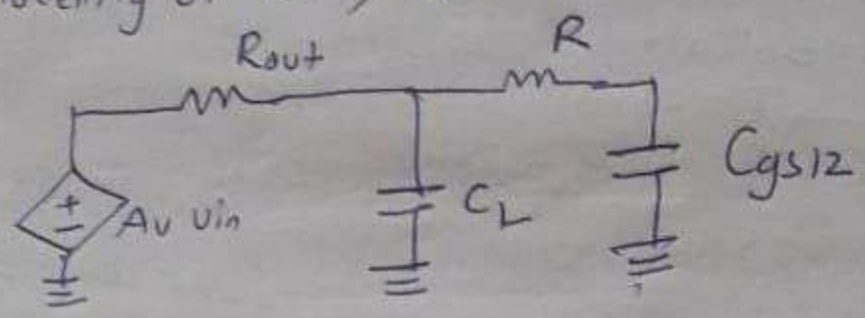
$M_{13}$: $W_{13} = (4 \times 8\mu m = W_3)$ → Same current (100μA)

↳ 1st order balancing is met.

The error amp. helps control 2nd order and PVT variation issues.

We have to ensure it's stability.

OUTPUT Modelling of Out1, Out2:




$C_{gs12} \gg C_L$

At dominant pole $C_{gs12}$ → open

$$P_1 = \frac{1}{R_{out} C_L}$$

↳ 2 poles, 1 zero

$UGF = A_v P_1$

↳ But more like single pole behaviour.

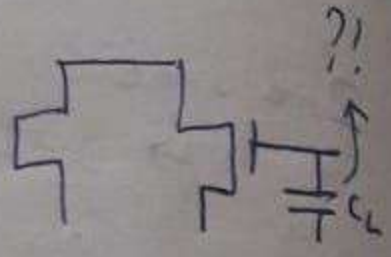
In feedback loop of error amp to M4 →

2nd pole = far away $\left( \frac{1}{g_{m13}} \Rightarrow R \Rightarrow p_2 = \frac{g_{m13}}{C_{gs13}} \right)$.

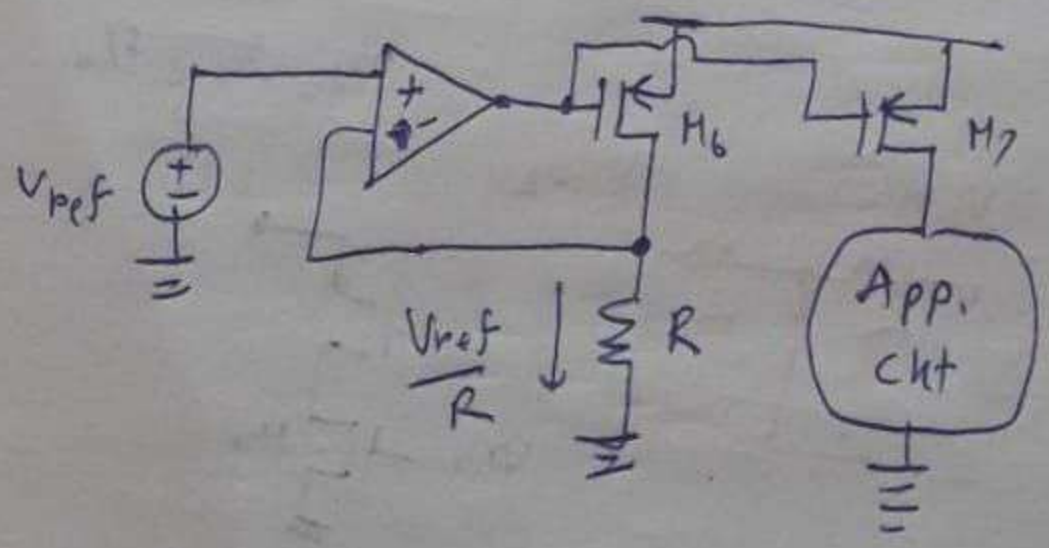
$p_2 = \frac{A(0)\, p_1}{\text{far}\,(90 - PM)}$

For this numeric take $C_{L1}, C_{L2} = 1pF$.

[Practise for test-3]




## Voltage to Current Conversion (Numeric)




OPAMP tunes $M_6$ to flow $\frac{V_{ref}}{R}$ through $M_7$

$M_6 \equiv M_7$

$M_6 \to 180°$ [We have to keep loop full phase 180]
to R

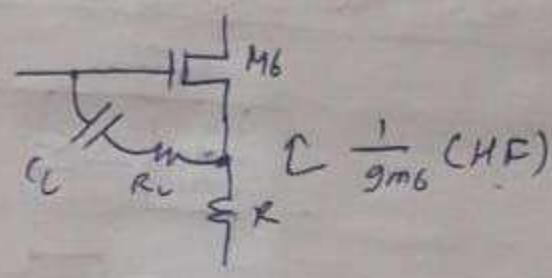
→ R to $M_3 \to 180°$ $M_3$ to $M_6 \to 180°$

$180° + 180° + 180° = 540° = 360° + 180° \to 180°$ [-ve feedback]

$$A_V = [g_{m1}(r_{o2} \| r_{o4})]\,[g_{m6}(r_{o6} \| R)]$$

1st stage

Pole at $G_{M6}$, $D_{M6}$ → If not far apart use Millen compensation




$\Big\downarrow \frac{1}{g_{m6}}$ (HF)

Value of $C_L$ to get reqd PM.

$$g_{m6} = \frac{\partial I_{sd6}}{\partial V_{sg6}}$$

[Maybe set as assign.]

$$\Delta V_{sg6} = \frac{\Delta I_L}{g_{m6}}$$

$\uparrow$

$\Delta V_{in} A_{V1}$

$$\Rightarrow \Delta V_{in} = \frac{\Delta I_L}{A_{V1} g_{m6}}$$

Q: $I_{sd6} = \frac{V_{ref}}{R}$ ? or $I_{sd3} = \frac{I_{DSS}}{2}$

↳ More dominant [see video - lost track]

Assuming gain of 1st stage is high

## Linear Regulator

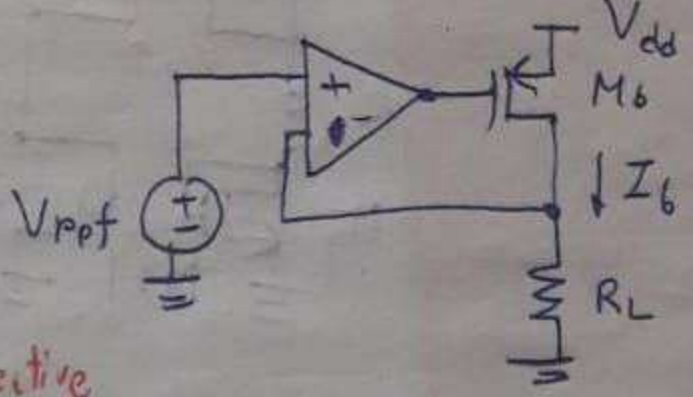
- Load regulation
- Line regulation

$V_{out}$ irrespective of $I_L$

$V_{out}$ irrespective of $V_{dd}$

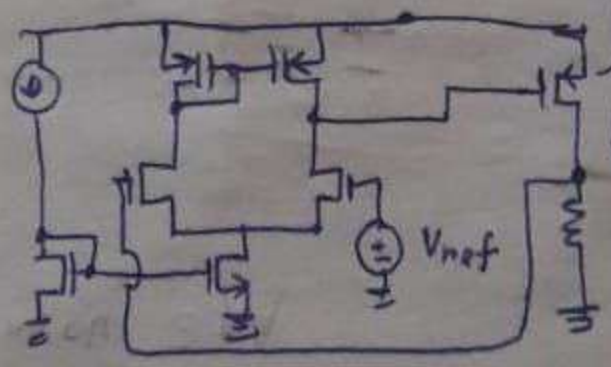
[Assuming control loop is successful]

min → 4 in triode
max → 2 in triode

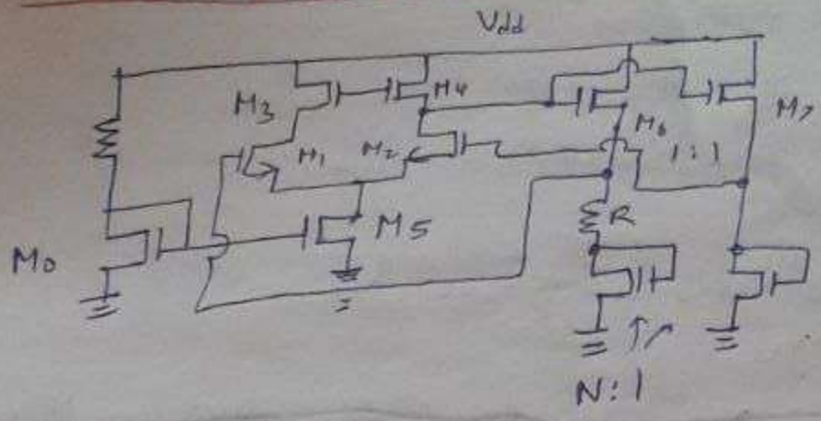



very big

Range of $I_{sd6}$: $I_{min}$ to $I_{max}$



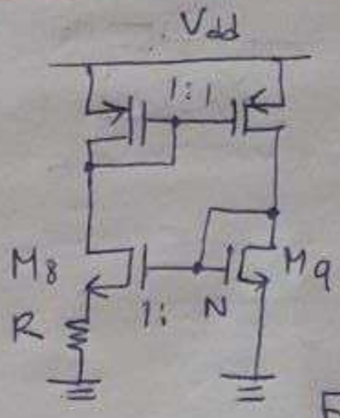
# Current Reference Circuit




10/11/20

# Current Reference Circuit

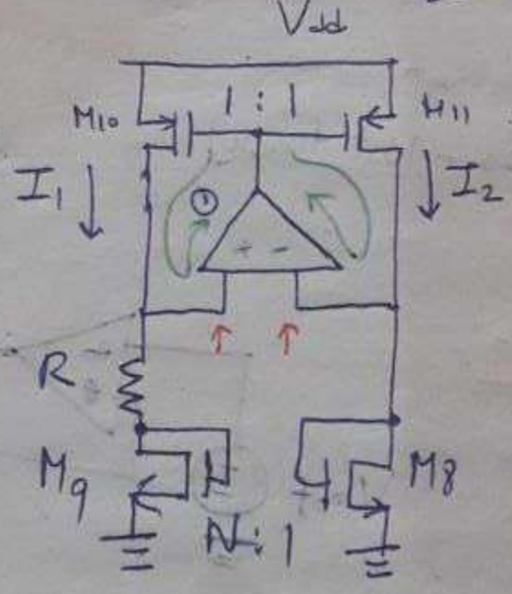
Earlier study:




$I \rightarrow$ function of $R, N$

$$I = \frac{1}{R^2}\left[\frac{2}{k_n' \frac{W_8}{L_8}}\right]\left[1 - \frac{1}{\sqrt{N}}\right]^2$$

Using OPAMP -




2 feedback paths

Same working principle as above circuit

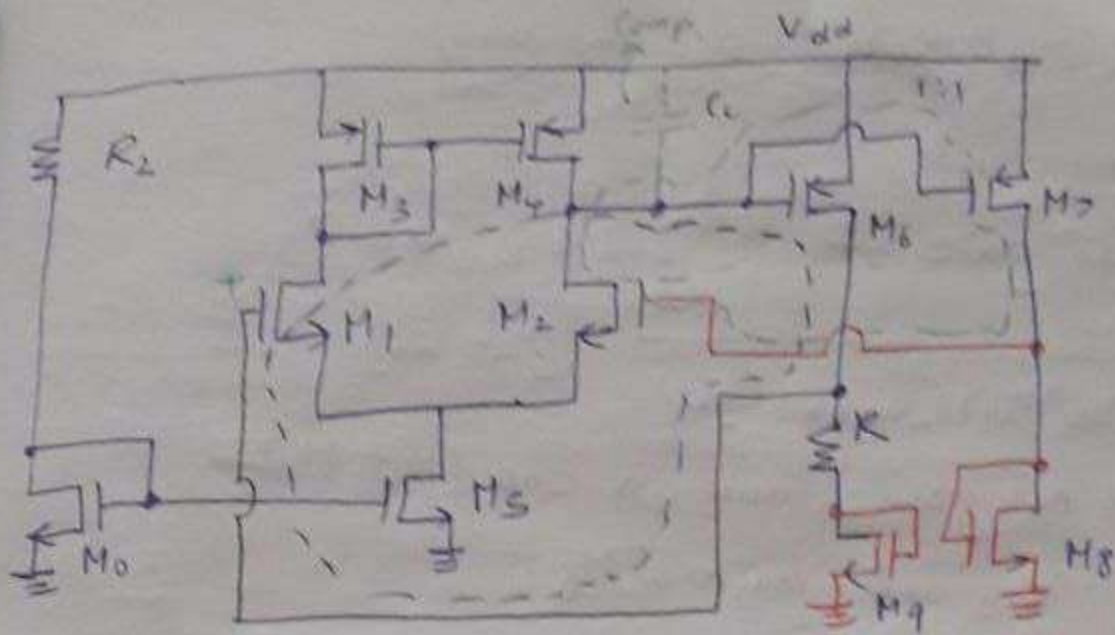
$\therefore I_1 = I_2$

OPAMP forces $V_{in1} = V_{in2}$

$\Rightarrow I_1 R + V_{GS9} = V_{GS8}$

[Same as above]

We now have to work only on the error amplifier




Left branch (see left page): [2nd diagram: Green line]

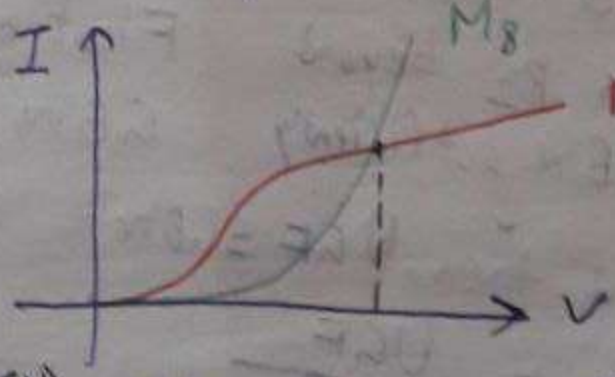
Loop Gain → $-A g_{m10}\left(R + \frac{1}{g_{m9}}\right)$ [A → Gain of error amp.]
(Left) ①

Loop Gain → $(-A)\left(-g_{m11} \cdot \frac{1}{g_{m8}}\right) = \frac{A g_{m11}}{g_{m8}}$
(Right) ②

Net gain of loop: $A g_{m10}\left[\frac{1}{g_{m8}} - \left(R + \frac{1}{g_{m9}}\right)\right]$
$[g_{m10} = g_{m11}]$

↓
Not sure whether dominating?!

Draw IV char of $M_8$ and $M_9$ on R [We want them to dominate]




* But still we have to check for OP-AMP stability.

slope of $M_8$ (IV) > Slope of $(M_9 + R)$

$\Rightarrow g_{m8} > \left(R + \frac{1}{g_{m9}}\right)$

$\Rightarrow \frac{1}{g_{m8}} < R + \frac{1}{g_{m9}}$

Same graph as in current ref. circuit

$\therefore$ Loop gain $< 0$ → Thus f/b is negative.

$A = g_{m1}(r_{o2} \| r_{o4})$ [Diff. amp gain]

Stability aspect:

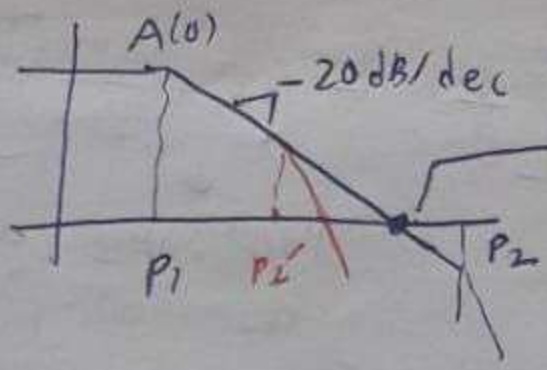
Pole at gate of $M_6$ and $D_6$ and $D_7$.

$$P_1 = \frac{1}{(r_{o2} \| r_{o4})(C_{gs6} + C_{gs7})}$$ [At G6]

If PM not good, add a cap. (Not Miller) at $V_{DD}$ and gate of $M_6$.

How to take current out? → Utilise Gate of $M_6$ ($V_{sg6}$) to bias PMOS and then propagate

In this Current Reference we have used $R_2$ in place of $I_{ref}$. $R_2$ has not much impact on performance of main circuit. Final I is determined by $M_6$, $M_7$, R.




→ Defines UGF even for 2nd order

~~UGF~~ GBW $= A(0)P_1$

[Single pole rolloff]

$P_2 > UGF$

↓

$GBW = UGF$

Find GBW

Push $P_2$ beyond GBW sufficiently

↓

And then $UGF = GBW$

$$P_2 = \frac{UGF}{\tan(90^\circ - PM)}$$

In case $P_2' < UGF$ →

First we pretend $P_2$ is beyond ~~UGF~~ GBW and then design $P_2$ as per PM. then declare GBW as UGF.

$$L.G = \frac{g_{m1}(r_{o2}\|r_{o4})\, g_{m6}}{[1+s(r_{o2}\|r_{o4})(2C_{gs6})]}\left[\frac{(\frac{1}{g_{m8}}\|r_{o7})}{1+s(\frac{1}{g_{m8}}\|r_{o7})(C_{gs8}+C_{gs2})} - \frac{(\frac{1}{g_{m9}}+R)\|r_{o6}}{1+s(\frac{1}{g_{m9}}+R)\|r_{o6}[C_{gs1}+C_{gd6}]}\right]$$

Add $C_c$ for pole compensation

↳ Left half zero $Z = P_2$

$$P_{r_{o6}} = \frac{1}{(r_{o2}\|r_{o4})(C_{gs6}+C_{gs7})}$$

$$P_{D_6} = \frac{1}{\left(r_{o6}\|\left(R+\frac{1}{g_{m9}}\right)\right)(C_{gd6}+C_{gs1})}$$

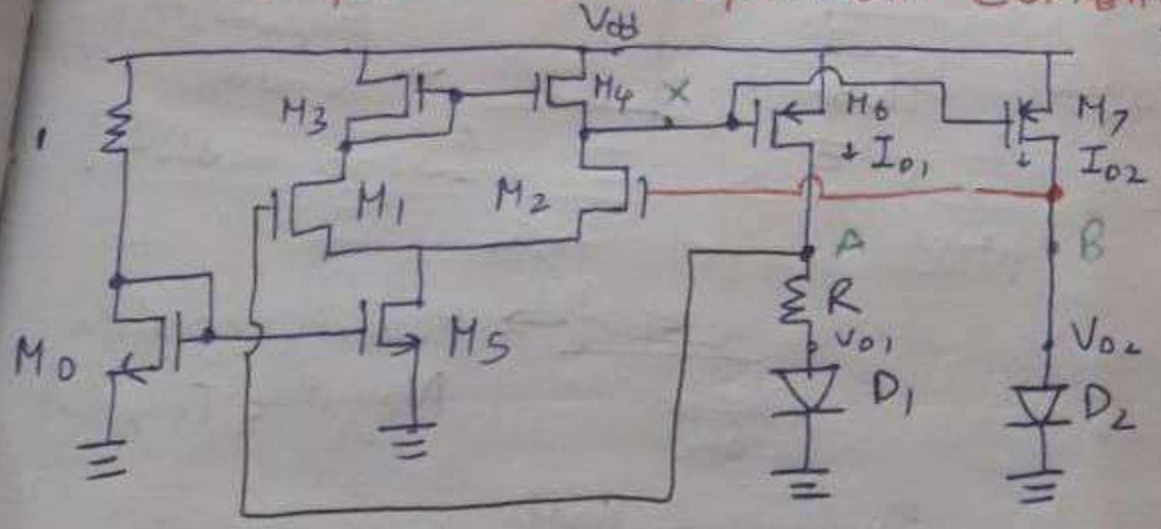
$C_{gd6}$ can be neglected

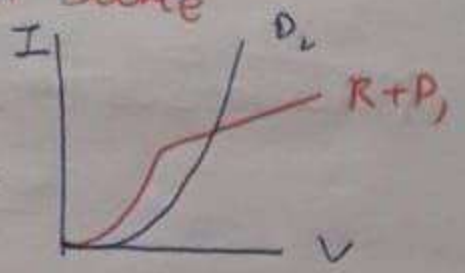
$$P_{D_7} = \frac{1}{\left(r_{o7}\|\frac{1}{g_{m8}}\right)(C_{gs8}+C_{gs2})}$$

Always consider capacitances in closed loop form.

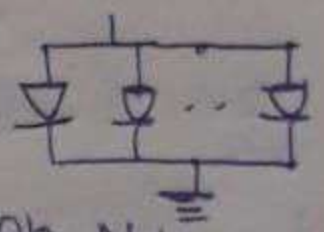
This circuit is immune to $V_{dd}$ fluctuations.

## □ Temperature Dependent Current Source




N: Number of diodes in parallel



Or N times junction area

$$D_2 \Rightarrow I_{D2} = I_0 \exp\left(\frac{V_{D2}}{V_T}\right)$$

$$D_1 \Rightarrow I_{D1} = N I_0 \exp\left(\frac{V_{D1}}{V_T}\right)$$

$$I_{D1} = I_{D2}$$

$$\Rightarrow V_{D2} - V_{D1} = V_T \ln(N)$$

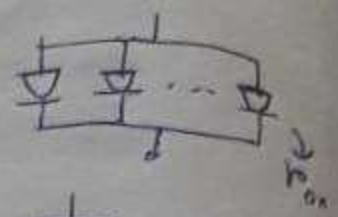
$$\Rightarrow \frac{V_{D2}-V_{D1}}{R} = \frac{V_T \ln(N)}{R} = I_{D1}$$ [Simpler than previous]

$$\frac{V_A}{V_x} = -g_{m6}\left[(R + r_{on1}) \parallel r_{o6}\right] \approx -g_{m6}(R + r_{on1})$$

$$\frac{V_B}{V_x} = -g_{m7}\left[r_{on2} \parallel r_{o7}\right] \approx -g_{m7} r_{on2}$$

$r_{on\_diode} \ll r_{o\_MOS}$

Thus by similar analysis the loop is stable.

$D_1$ : 

$D_2$ :

$$I_D = I_0 \exp\left(\frac{V_D}{V_T}\right)$$

$$\Rightarrow r_{on} = \left[\frac{\partial I_D}{\partial V_D}\right]^{-1} = \frac{I_D}{V_T}$$

$$r_{on1} = \frac{V_T}{I_{D1}}$$

$$r_{on2} = \frac{V_T}{I_{D2}}$$

$\rightarrow r_{on1} = r_{on2}$

$$I_D = \frac{V_T \ln(N)}{R}$$

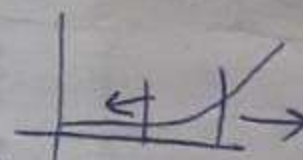
$$= \frac{kT}{qR}\ln(N)$$

$I_D$ is strongly dependent on T

Assume $\frac{\partial R}{\partial T} = 0$

MOS in subthreshold → Exponential char.

[Same as diode]

MOS  → Mobility degradation

Negative Temp. Coeff

Carrier gen.

Positive Temp. Coeff. (like diodes)

In application circuits, we use BJT in place of diodes.

npn

$$I_C = I_0 \exp\left(\frac{V_{BE}}{V_T}\right)$$

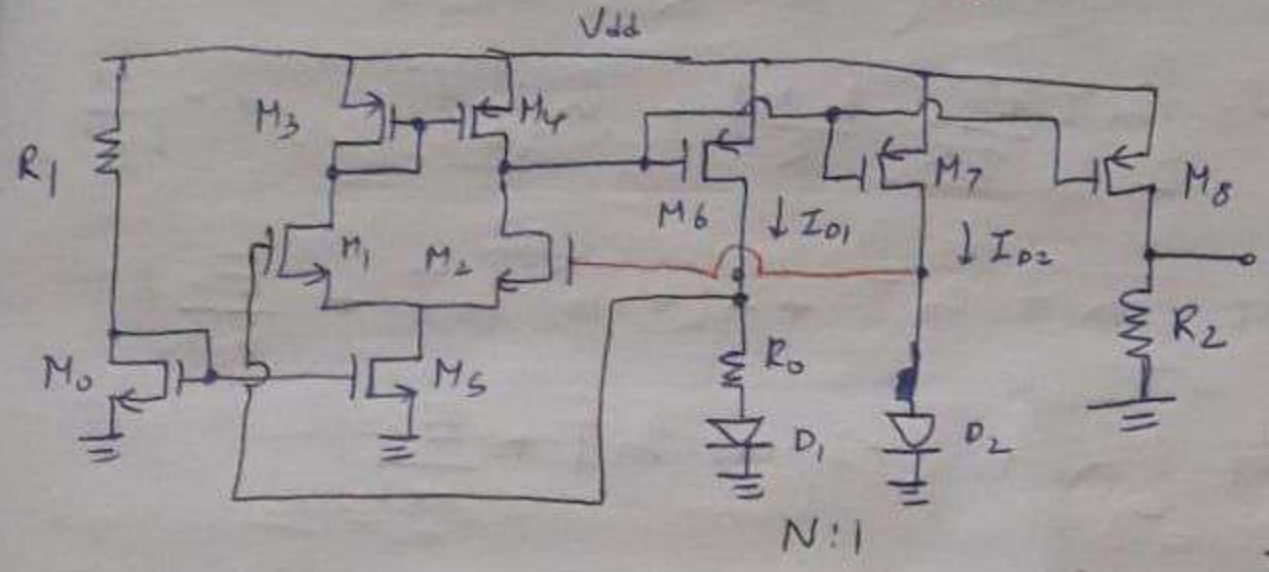
pnp

Node X → dominant pole [3 dB BW]

poles A, B → Very far away [R eq at nodes are quite]

## Voltage Reference Circuit

□ Temperature dependent voltage.



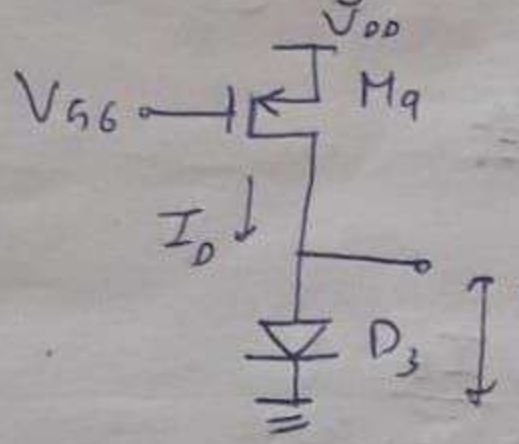

$V_o = R_2 I_{D1}$

$= \frac{R_2}{R_0} \ln(N) V_T$

↳ +ve Temp. Coeff

$I_{D1} = I_{D2}$

If we pass through another diode the same current $I_{D1}$




(Strong temperature dep.)

↓

May not have same dependence as $V_o$

[$R_2$, $D_3$ → diff temp. dep.]

$I_D = I_0 \exp\left(\frac{V_{D3}}{V_T}\right)$

~~$V_{D3} = V_T \ln\left(\frac{I_D}{I_0}\right)$~~

~~$= V_T \ln\left(\frac{1}{R}\right)$~~

$I_D = I_{D1} = I_{D2} = \frac{V_T \ln(N)}{R}$

$\frac{\partial I_D}{\partial T} = \frac{\partial}{\partial T}\left(\frac{kT}{q}\frac{\ln N}{R}\right)$

$= \frac{k}{q}\frac{\ln N}{R} = \frac{I_D}{T}$

$I_0 = b T^{4+m} e^{-\frac{E_g}{kT}}$

$$I_{D3} = I_0 \exp\left(\frac{V_{D3}}{V_T}\right)$$

$$\Rightarrow \quad V_{D3} = V_T \ln\left(\frac{I_{D3}}{I_0}\right)$$

$$= V_T \ln\left(\frac{V_T \ln N}{R} \cdot \frac{1}{b} T^{-(4+m)} \exp\left(+\frac{E_g}{k_B T}\right)\right)$$

$$= V_T \left[\ln\left(\frac{kT}{qR} \cdot \frac{\ln N}{R}\right) + \ln\left(\frac{1}{b} T^{-(4+m)}\right) + \frac{E_g}{k_B T}\right]$$

$$= V_T \left[\alpha + \ln T + -(4+m) \ln T + \frac{E_g}{k_B T}\right]$$

$$= V_T \left[\alpha + (-3-m) \ln T + \frac{E_g}{k_B T}\right]$$

$$\frac{\partial V_{D3}}{\partial T} = V_T \left[\frac{(-3-m)}{T} + \frac{E_g}{k_B T^2}\right]$$

$$+ \frac{k}{q} \ln\left(\frac{I_{D3}}{I_0}\right)$$

$$\frac{\partial V_D}{\partial V_T} = \frac{\partial}{\partial T}\left\{\frac{kT}{q} \ln\left(\frac{I_D}{I_0}\right)\right\}$$

$$= \frac{k}{q} \ln\left(\frac{I_D}{I_0}\right) + \frac{kT}{q} \cdot \frac{I_0}{I_D}\left[\frac{I_D' \cdot I_0 - I_0 \cdot I_0'}{I_0^2}\right]$$

Fresh: $I_D = I_0 \exp\left(\frac{V_D}{V_T}\right)$

$I_0 = b\,T^{(4+m)} \exp\left(\frac{-E_g}{kT}\right)$

$$\Rightarrow \frac{\partial I_0}{\partial T} = (4+m)\frac{I_0}{T} + \frac{E_g}{kT}\cdot\frac{I_0}{T}$$

$$V_D = V_T \ln\left(\frac{I_D}{I_0}\right)$$

$$\Rightarrow V_D = \frac{kT}{q}\ln\left(\frac{I_D}{I_0}\right)$$

$$\Rightarrow \frac{\partial V_D}{\partial T} = \frac{\partial}{\partial T}\left\{\frac{kT}{q}\ln\left(\frac{I_D}{I_0}\right)\right\}$$

$$= \frac{k}{q}\ln\left(\frac{I_D}{I_0}\right) + \frac{kT}{q}\frac{I_D}{I_D}\left[\frac{1}{I_0}\frac{\partial I_0}{\partial T} - \frac{I_0}{I_0^2}\frac{\partial I_0}{\partial T}\right]$$

$$= \frac{V_D}{T} - (4+m)\frac{kT}{qT} - \frac{E_g/q}{T} + \frac{kT}{q}\cdot\frac{1}{T}$$

↓ Dominant

Si → $m = -1.5$

Final expression:

$$\frac{\partial V_D}{\partial T} = \frac{V_D}{T} - \underbrace{(3+m)\frac{V_T}{T}}_{\text{small}} - \frac{E_g/q}{T}$$

→ Cancellation is only at 1 temp.

$V_D$: 0.6–0.7 V

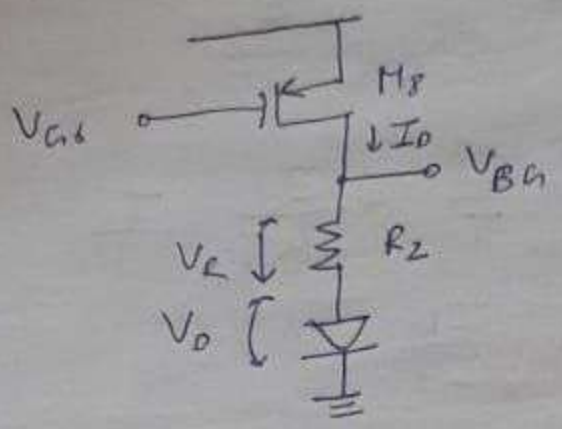
$\frac{E_g}{q}$: 1.12 V (Si)

Thus $\frac{\partial V_D}{\partial T}$ is -ve.

Voltage dependency at diode → -ve

Voltage dependency at resistor → +ve

Combine two opposite current coefficent → cancel them (temp. independent)




Tune $R_2$ so that $V_R$ and $V_D$ temp. coeff are equal and opposite

$\left[\because \frac{\partial V_{BG}}{\partial T} = 0\right]$

$$V_{BG} = I_D R_2 + V_D$$

$$\frac{\partial V_{BG}}{\partial T} = 0$$

$$\Rightarrow R_2 \frac{\partial I_D}{\partial T} + \frac{\partial V_D}{\partial T} = 0$$

$$I_D = I_0 \exp\left(\frac{V_D}{V_T}\right)$$

$$\because I_D = \frac{R_2}{R_0} \ln(N) V_T$$

$$\frac{\partial I_D}{\partial T} = \frac{1}{R_0} \ln(N) \frac{V_T}{T}$$

$$\Rightarrow \frac{R_2}{R_0} \ln(N) \frac{V_T}{T} + \frac{V_D}{T} - (3+m)\frac{V_T}{T} - \frac{(E_g/q)}{T} = 0$$

Set the circuit and set $I_D$.
Find value so that we have operation $\frac{\partial V_{BG}}{\partial T} = 0$ at our desired temp. → Find $V_D$ [will be given]

Either $I_D$ or $V_D$ has to be there.

Replace T by 300K

$V_T \approx 26mV$

$m = -3/2$

$\frac{E_g}{q} = 1.12\ V$

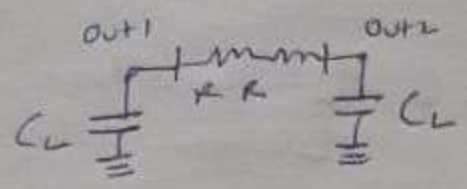
Thus we get $R_2/R_0$ for zero temp. coeff.

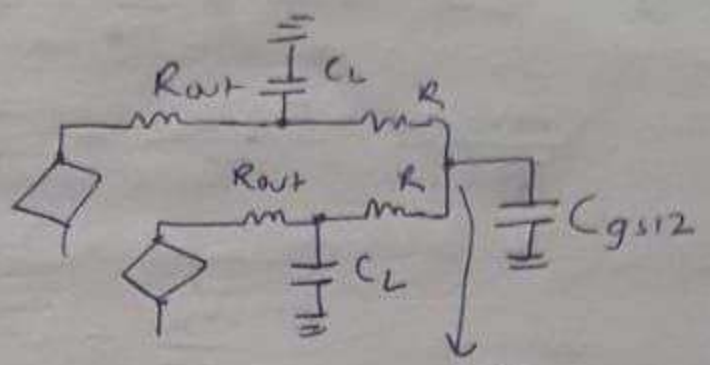
Used as precision voltage reference [$V_{BG}$ will be close to $\frac{E_g}{q}$]

For $V_{dd} < 1.12V$
↓
Low voltage
Bandgap circuits.

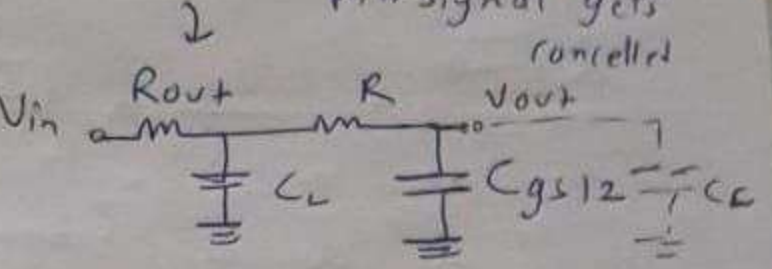
Hence called
BANDGAP
REFERENCE
CIRCUIT

CMFB Doubt




Diff signal gets cancelled




R has to be atleast Rout to avoid loading.

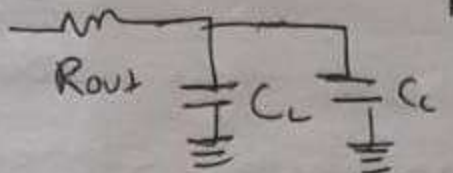
R, Rout → same order

$C_L$ → no control of poles of 2stage OTA

$C_{gs12}$ → put extra Cap

2 poles, 1 zero

If $C_C \gg C_L$

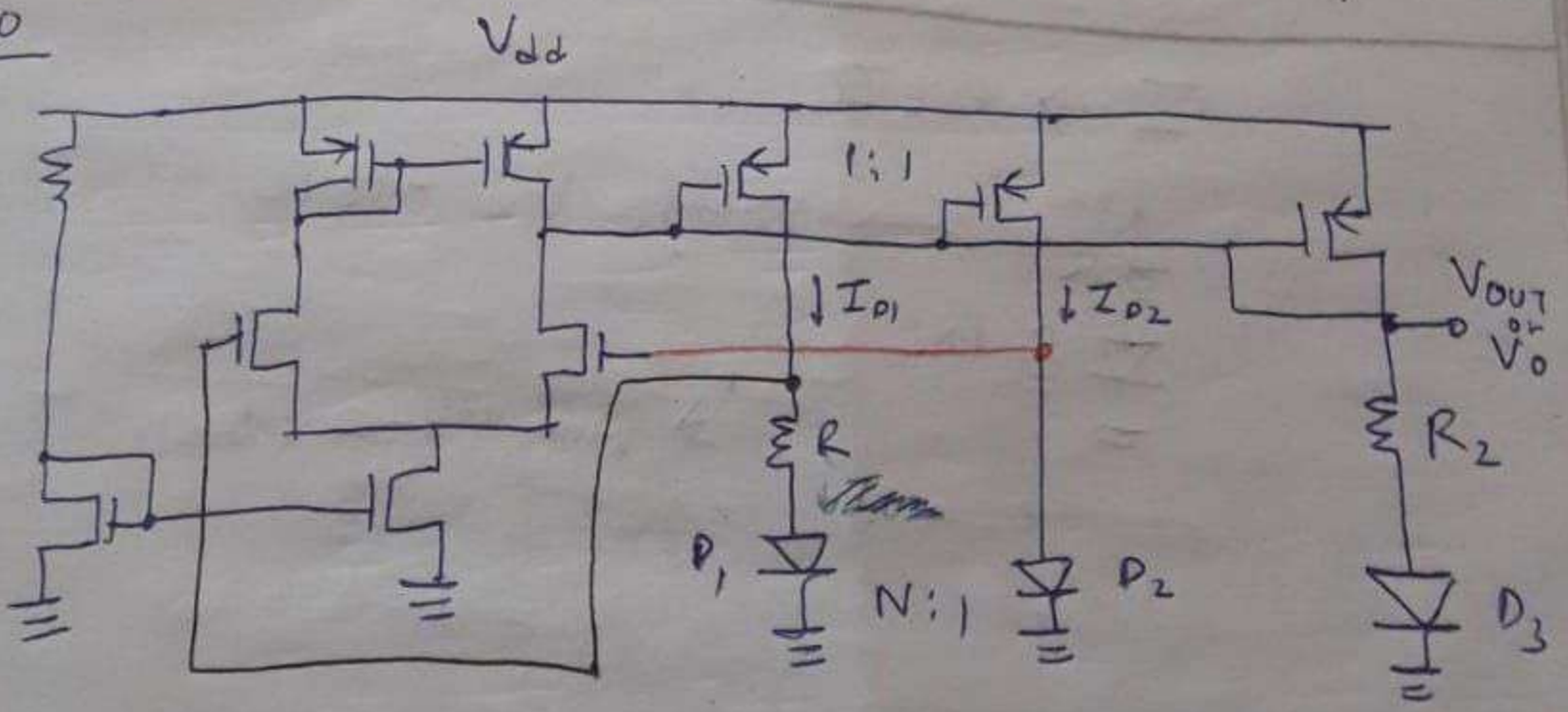



$$\frac{1}{R_{out}(C_L + C_C)}$$

2 Dominant pole

* Some issues in formulae (one possibility)
↳ Will be mentioned in subsequent class.

12/11/20




$$I_{D1} = \frac{V_T \ln(N)}{R}$$

$$\frac{\partial I_{D1}}{\partial T} = \frac{I_{D1}}{T}$$

$$V_O = I_{D1} R_2 + V_{D3}$$

$$V_o = V_T \ln N \cdot \frac{R_2}{R_0} + V_{D3}$$

$$\frac{\partial V_o}{\partial T} = \frac{R_2 I_{D1}}{T} + \frac{\partial V_{D3}}{\partial T} = 0 \quad \begin{matrix}[\text{indep. of temp}\\ [0 \text{ Temp. Coeff}]\end{matrix}$$

$$\downarrow$$

$$\frac{V_{D3}}{T} - (3+m)\frac{V_T}{T} - \frac{(E_g/q)}{T}$$

$$\frac{R_2 \overset{I_{D2}}{\overset{\shortparallel}{I_{D1}}}}{T} + \left(\frac{V_{D3}}{T} - (3+m)\frac{V_T}{T} - \frac{(E_g/q)}{T}\right) = 0$$

$$\Rightarrow R_2 = \frac{(3+m)V_T + \frac{E_g}{q} - V_{D3}}{I_{D1}}$$

Numerically plugging $R_2$ in $V_o \rightarrow$ we get $V_o \approx \frac{E_g}{q}$

$V_o \approx 1.12V \Rightarrow V_{DD} > 1.12V$

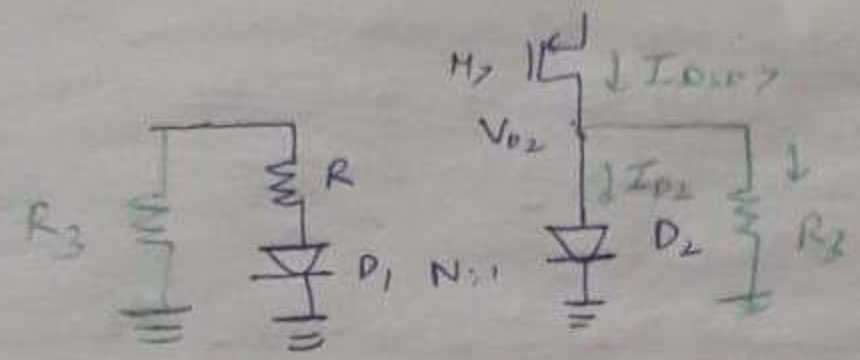
↳ Not useful if $V_{DD} < 1.12V$

Rather than adding voltages $R_2, D_3$ we can add currents,

$I \rightarrow$ +ve TC.

$\longrightarrow$ Voltage $V_x$ -ve TC

↳ Add the (Current)




$$I_{SD7} = I_{D2} + V_{D2}/R_3$$

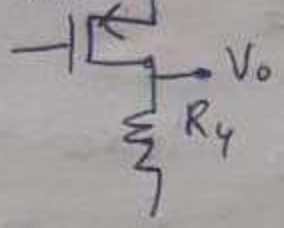
$$\Rightarrow \frac{\partial I_{SD7}}{\partial T} = \frac{\partial I_{D2}}{\partial T} + \frac{1}{R_3}\frac{\partial V_{D2}}{\partial T}$$

$$\hookrightarrow \left(\frac{V_{D2} - (3+m)V_T - E_g/q}{T}\right)$$

$$\Rightarrow \frac{\partial I_{SD7}}{\partial T} = \frac{I_{D2}}{T} + \frac{1}{R_3}\left[\frac{V_{D2} - (3+m)V_T - E_g/q}{T}\right] = 0$$

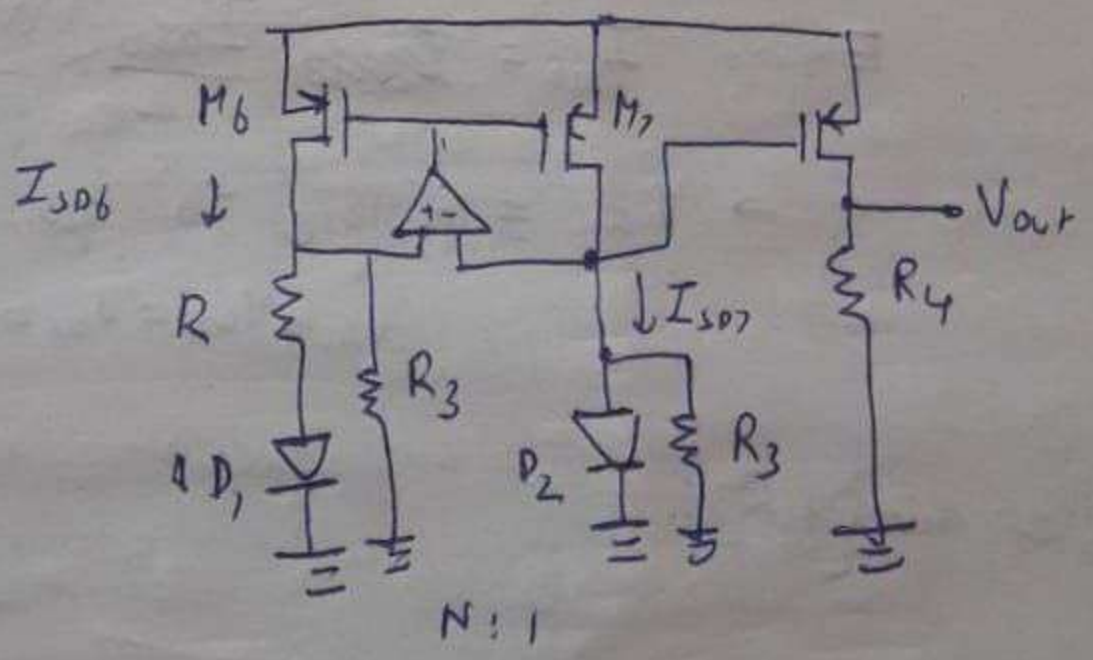
Find $R_3$ from here [0 TC]

↳ Advantage → No need for 3rd ~~—M—▷|—~~ in brand
→ Simply put resistor at output




$I_{D57}$ has 0 TC.
It is mirrored to $M_8$ and hence $V_o$ is 0 TC.
However $V_o$ need not be 1.12V It can be anything.

This design is called low voltage bandgap ref. circuit. ←



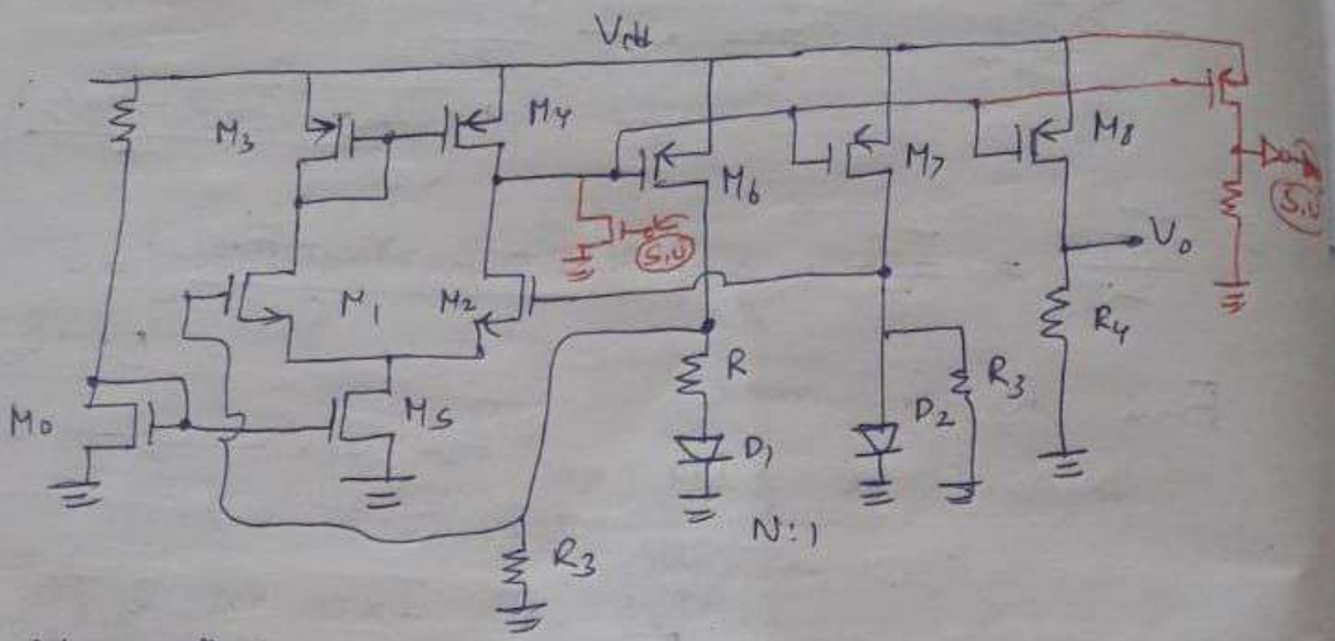

$I_{SD6} = I_{SD7}$

↳ 0 TC.

Even after adding $R_3$, the net relative impedance [earlier $(R+r_{o,1})$ and $(r_{o,2})$] remains same. So -ve f/b is maintained only loop gain changes.

$$[g_{m6}(R_3 \parallel (R+r_{onD1}) \parallel r_{o6}) - g_{m7}(r_{on2})]\, A_d$$

WORD OF CAUTION: (Low Voltage BG Ref.)




$V_{D2} \sim 0.6V$

ICMR of diff amp lower limit $< 0.6V$

↳ Make $I_{bias}$ of ICMR small

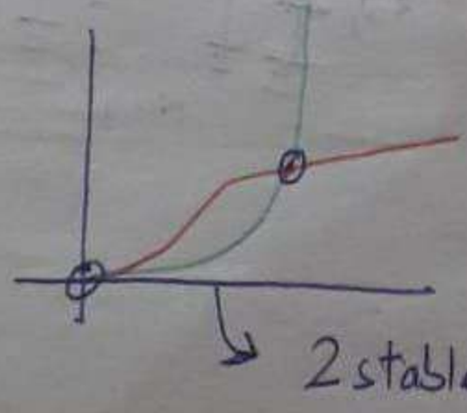
$V_{GS1} + V_{dsat5} < V_{D2}$

Ensure $I_{SD6} = \cancel{I_{bias}}\ \frac{I_{DSS}}{2} \times \frac{(W/L)_6}{(W/L)_3}$ [Current mirror]

→ $V_{G1} \equiv$ Close to quiscent voltage.

$V_{G1} = V_{G2} = V_{D2} = 0.6V$

Even after adding $R_3$:



Initially if $I_6 = I_7 = 0$ even after $M_6$ is on, $V_{B2}$, $I_R \cdot V_{B1} = 0$ → Startup issue again
→ $I_6 = I_7 = 0$

This circuit has Startup issue after adding $R_3$s.

Solution → Same as current ref (Marked red in left page)
[Only 1 inverter]

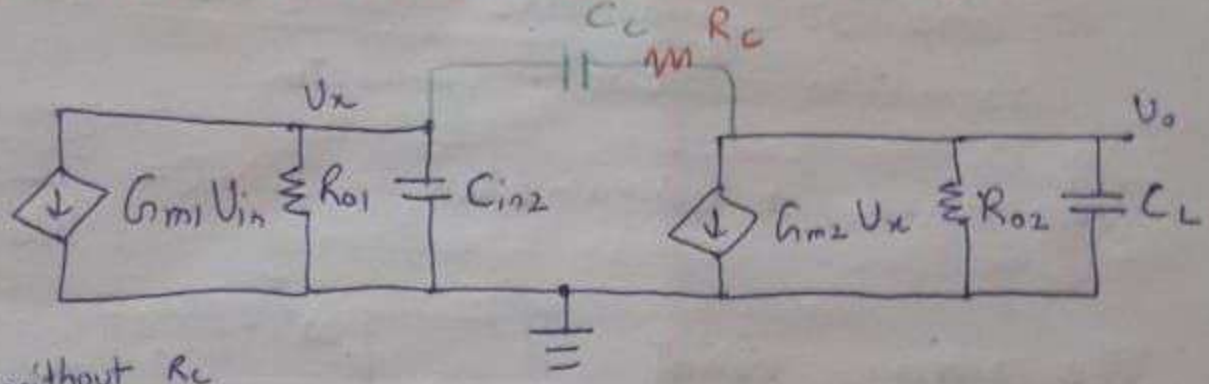
↳ Current is pulled through $M_4$

Sometimes $\frac{\partial R}{\partial T} \neq 0$.

If we have manged to make $\frac{\partial V_o}{\partial T} = 0$ but $\frac{\partial R_4}{\partial T} \neq 0$, then $\frac{\partial V_o}{\partial T} \neq 0$.

Thus we have to make $I_{SD7}$ having non-zero T.C. so that $\frac{\partial R_4}{\partial T}$ and $\frac{\partial I_{SD8}}{\partial T} = \frac{\partial I_{SD7}}{\partial T}$ cancel to give $\frac{\partial V_o}{\partial T} = 0$.

## * Location of Poles and Zeros in 2stage OPAMP.




Ignore earlier formulae

without $R_c$

$$P_1 = \frac{-1}{R_{o1}(G_{m2} R_{o2} C_c + C_c + C_{in2})} \approx \frac{-1}{R_{o1} G_{m2} R_{o2} C_c} \quad \text{(LHP)}$$

$$P_2 = \frac{-G_{m2}}{\left(C_L + C_{in2} + \frac{C_L}{C_c} C_{in2}\right)} \approx \frac{-G_{m2}}{C_L + C_{in2}} \quad \text{(LHP)}$$

$$Z = \frac{G_{m2}}{C_c} \quad \text{(RH plane)}$$

with $R_c$

$P_1$ → same

$P_2$ → slight change (for numeric sake)

$$Z = \frac{1}{C_c\left(\frac{1}{G_{m2}} - R_c\right)}$$

↳ Pushto $\infty$ $\left[R_c = \frac{1}{G_{m2}}\right]$

$$P_3 = \frac{1}{R_c C_c} = \frac{G_{m2}}{C_c}$$

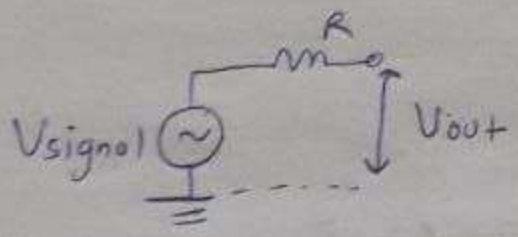
Week-12 (Final week)

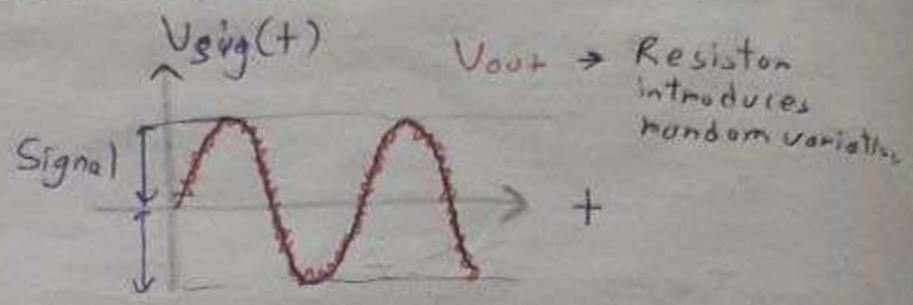
16/11/20

# NOISE ANALYSIS

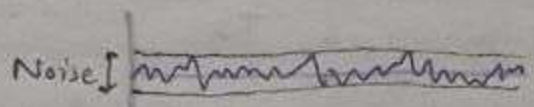
## Introduction: Noise Source

- Effect of noise:




Vsig vs Vout




Unwanted fluctuation

More fluctuation → poorer signal quality

↓ cause

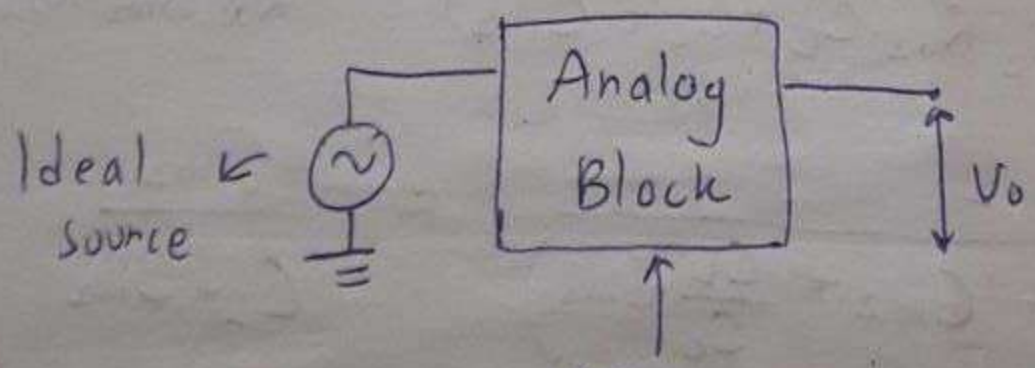
Resistor

If amp. of signal and noise are comparable, information is badly corrupted.

We have a parameter $SNR = \frac{\text{Signal strength}}{\text{Noise strength}}$ ∴

↕ quality of signal.

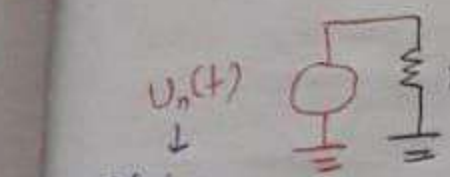
We always want high SNR.




No option to get rid completely.

- Measurement of noise strength.

Higher $|U_n(t)|$, more $P_{diss}$ across $R_L$.




$$\lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \frac{U_n^2(t)}{R_L}\, dt = P_{av} \quad (W)$$

→ Average Noise power

$T \to \infty$ wrt. noise voltage duration (?)

↓ But it depends on $R_L$

RF Guys: $R_L = 50\Omega$

Analog and RF Guys: $R_L = 1\Omega$ (Normalized)

- Normalised noise power:

Normalised wrt. $R_L$ ⇒

$$P_{av\,(norm)} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} U_n^2(t)\, dt \quad (V^2)$$

↳ Normalised average noise power

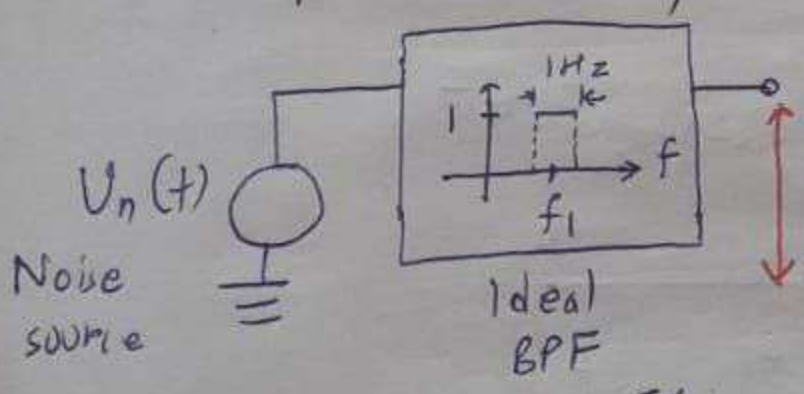
Once $P_{av\,(norm)}$ is known, given $R_L \rightarrow P_{av} = \frac{P_{av\,(norm)}}{R_L}$

Is the noise smooth or rapidly changing? [Freq. characteristics]

$P_{av}$ captures only amplitude part.

## Noise Power Spectrum (Noise characterization)

- Power spectral Density




$$\lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \hat{U}_n^2(f_1, t)\, dt = P_{av}(f_1)$$

↳ we drop it

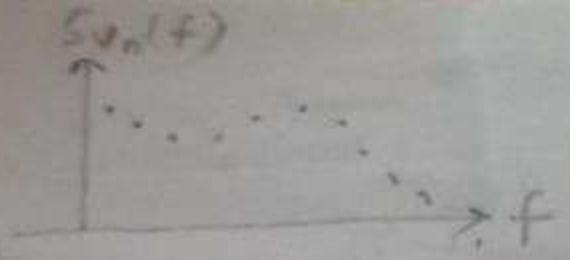
↳ $S_{U_n}(f)$

Density of strength at $f_1$ in a small interval

↳ $S_{U_n}(f)$

Spectral density of $U_n(t)$

Unit: $(V^2/Hz)$




→ Noise has low and mid frequency components.

- Equivalent voltage density

$S_{V_n}(f) \rightarrow V^2/Hz$

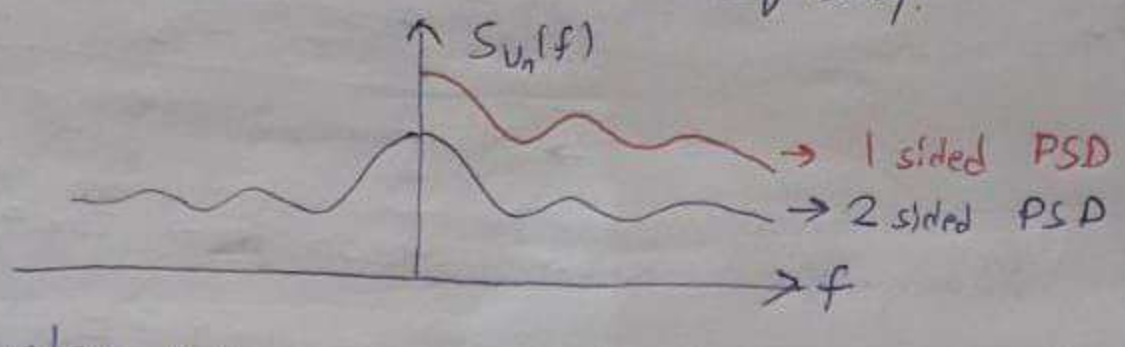
Convent to voltage → $\sqrt{S_{V_n}(f)} \rightarrow V/\sqrt{Hz}$

[Sometimes also said as PSD]

↳ Be careful, it is actual VSD

Voltage Spectral Density. ≡ VSD

We have a notion of -ve frequency.




For analog purpose, we fold it to +ve f axis only.

↳ One sided power spectrum

Total ~~signal~~ noise strength = $\int_0^{\infty} S_{V\,(one\text{-}sided)}(f)\,df$

$\int_{-\infty}^{\infty} S_{V\,(2\text{-}sided)}(f)\,df$

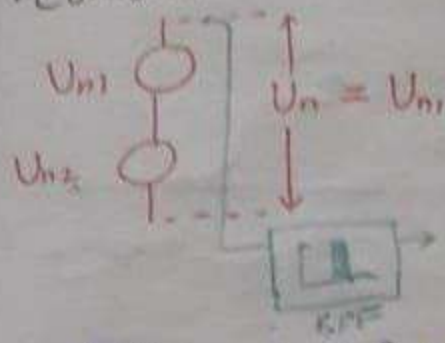
$$P_{total} = \int_0^{\infty} S_{V_n}(f)_{O.S.\,PSD}\,df$$

$(V^2)$ or $P_{ov}$

VSD: (rms of PSD) = $\sqrt{\lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \hat{U}_n^2(f,t)\,dt}$

# Cumulative effects of multiple noise sources

- Correlated and Un-correlated noise-sources




Filtering of all 3 ports

→ Characteristic of total noise

$$V_n^2 = (V_{n1} + V_{n2})^2 dt$$

$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} (V_{n1} + V_{n2})^2 dt$$

(overall)

$V_{n1}^2 dt$ $\quad$ $V_{n2}^2 dt$ $\quad$ $2V_{n1}V_{n2} dt$

$$P_{av} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} V_{n1}^2 + V_{n2}^2 + 2V_{n1}V_{n2}\, dt$$

$V_{n1}^2$ → Source1 noise → After filtering $P_{av}$ → $S_{Vn1}(f)$

$V_{n2}^2$ → Source2 noise → $S_{Vn}(f)$

$2V_{n1}V_{n2}$ → Uncorrelated → 0
Correlated ≠ 0
↓
0 [In most cases]

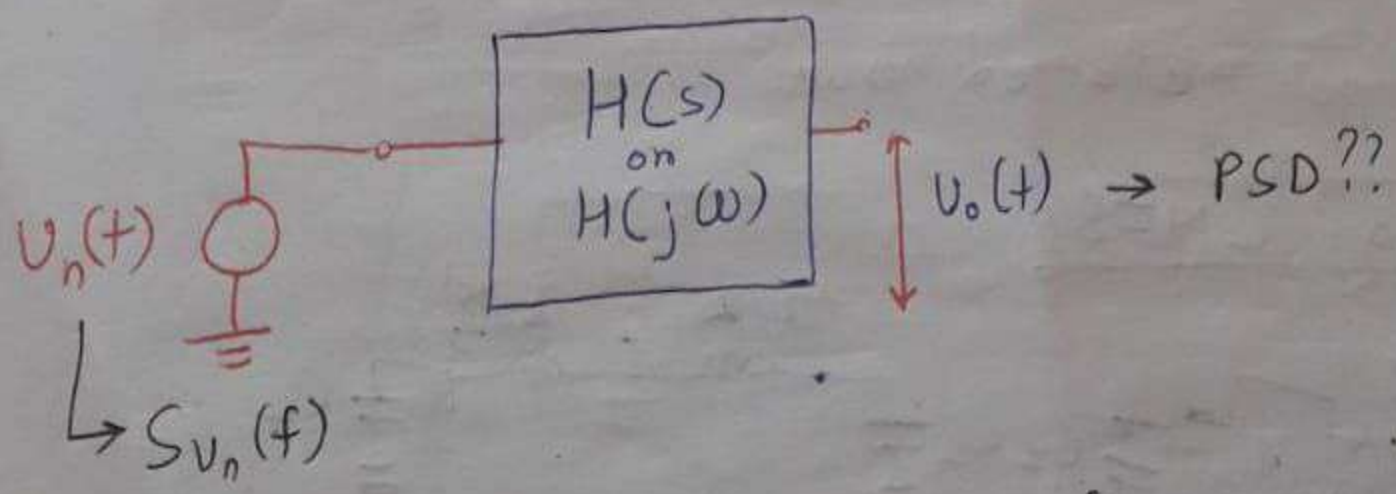
- Overall PSD of uncorrelated noise sources:

$$S_{V_{net}}(f) = S_{Vn_1}(f) + S_{V_{n2}}(f)$$

$$\sum_{i=1}^{N} S_{Vn_i}(f) = S_{V_{net}}(f)$$

# Noise through a System (Shaping)

## Shaping of PSD of noise sources

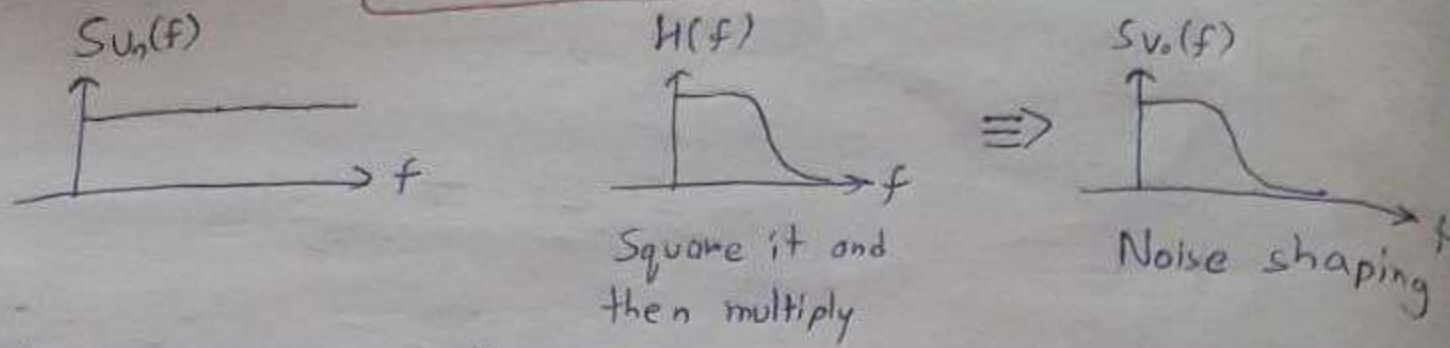



$$S_{V_o}(f) \Rightarrow \int \{V_n(t) \circledast h(t)\}^2 dt$$

↳ Time domain

For complex numbers ⟶ $|H(j\omega)|^2$

$$S_{V_o}(f) = S_{V_n}(f)\ |H(f)|^2$$

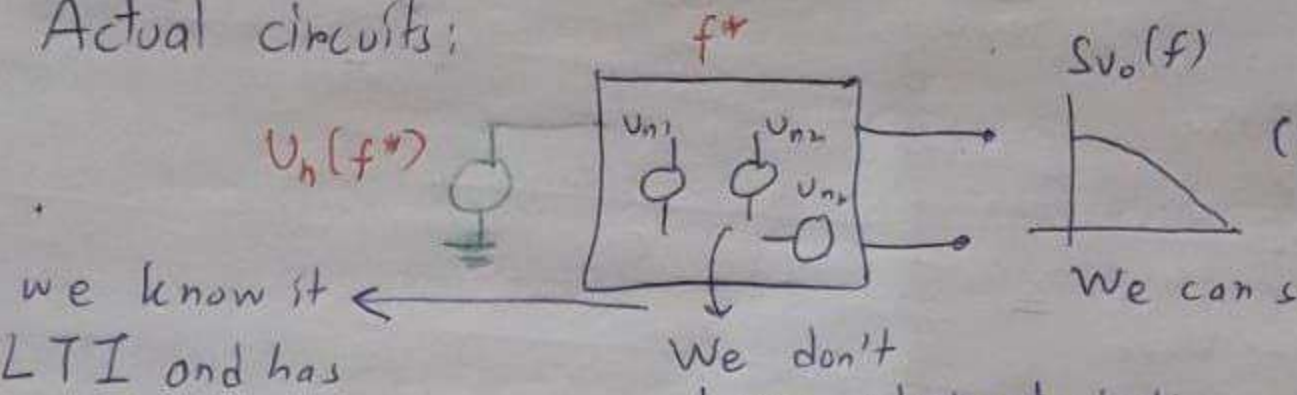



We can reverse the process.

We know $S_{V_o}(f)$ and want to know $S_{V_n}(f)$

$$S_{V_n}(f) = \frac{S_{V_o}(f)}{|H(f)|^2}$$

Actual circuits:




If we know it is LTI and has an $H(jf)$

We can see this

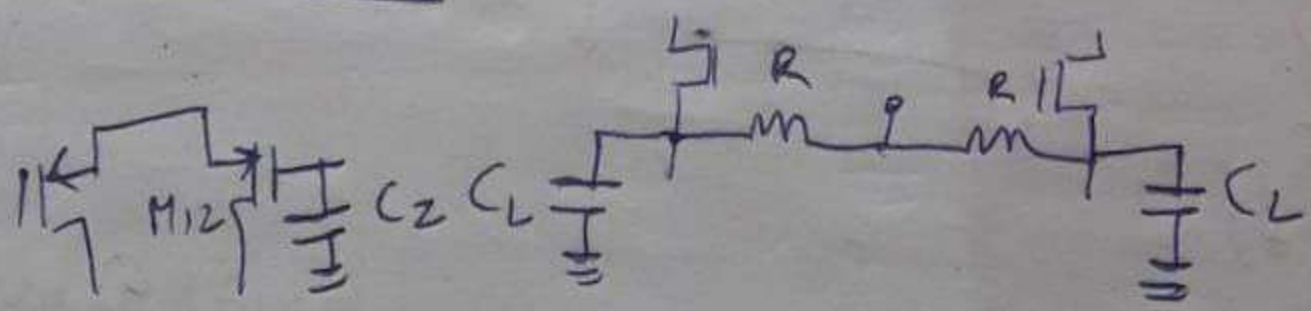
We don't know characterisation

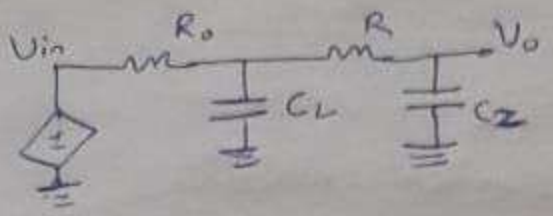
$$\rightarrow S_{V_n}(f) = \frac{S_{V_o}(f)}{|H(f)|^2} \rightarrow$$ Modelling equivalent noise source

People prefer to combine all noise source effects and characterise it at $f^*$ and model it as equivalent noise source at input.

↳ Input referred noise.

## Note on CMFB






We want poles of this circuit.
Assuming $C_2$ large enough.

$$\frac{V_o}{V_{in}} = \frac{1}{(1 + s(RC_2 + R_0(C_L + C_2)) + s^2(R_0 R C_L C_2))}$$

↳ 2 poles

Dominant pole: $P_1 = \frac{1}{(R + R_0)C_2}$ → ($C_L$ open at low freq)

(coming from $C_2$)

We can easily compensate by choosing big $C_2$.

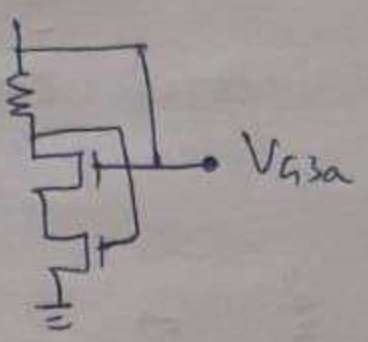
$$P_2 = \frac{1}{(R_0 \| R_0) C_L}$$

↳ ($C_2$ short at high freq)

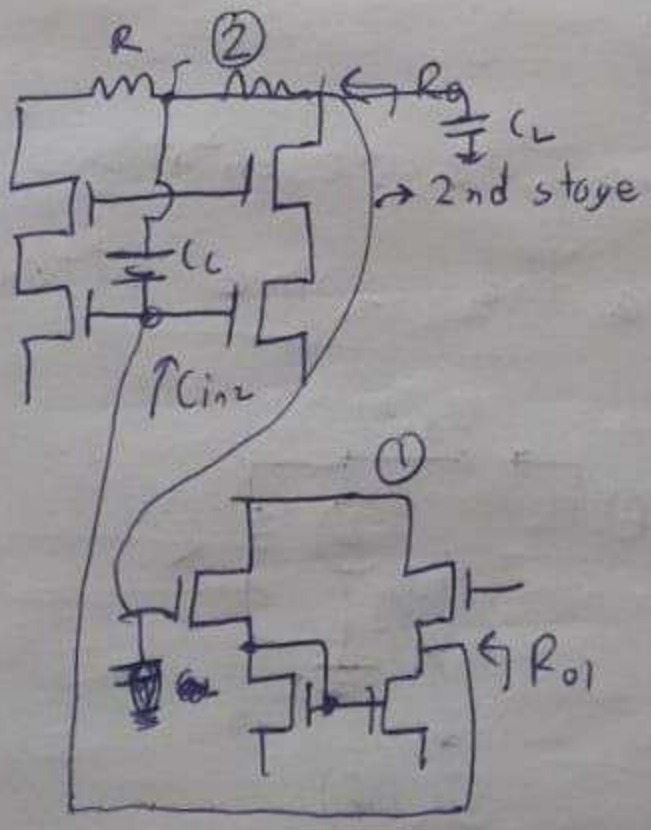
Gain of circuit = $\frac{g_{m12}}{g_{m13}}$ (1st stage)

$V_{G1a}$, $V_{G3a}$ → Seperate circuits to deploy voltage

→ Use wide swing cascode




We can do diff. pole compensation




(Miller effect)

$$P_1' = \frac{1}{(C_C G_{m2} R_{o2}) R_{o1}}$$

$$P_2' = \frac{G_{m2}}{C_L + C_{in2}}$$

$$Z = \frac{1}{RC_C} \text{ (LHP)}$$

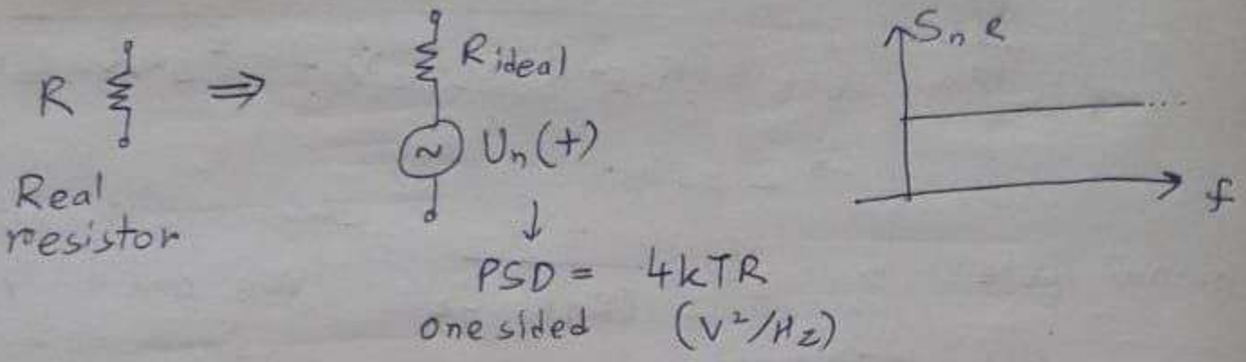
$$P_3 = \frac{1}{RC_C}$$

Pole zero cancellation

17/11/20 (Last Lecture)

## Noise Sources in Circuits

- Resistor (Voltage, Current source)




$\downarrow$

PSD = $4kTR$ one sided $(V^2/Hz)$

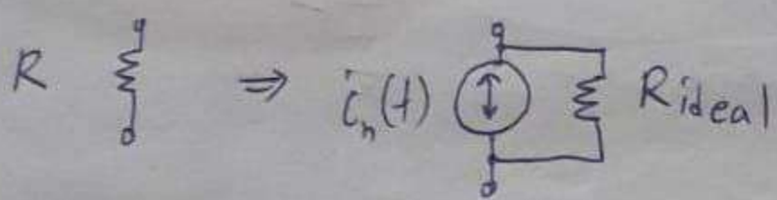
Is it constant for entire freq.?

$$P_{av} = \int_0^{\infty} 4kTR \, df = \infty$$

Practically not the case

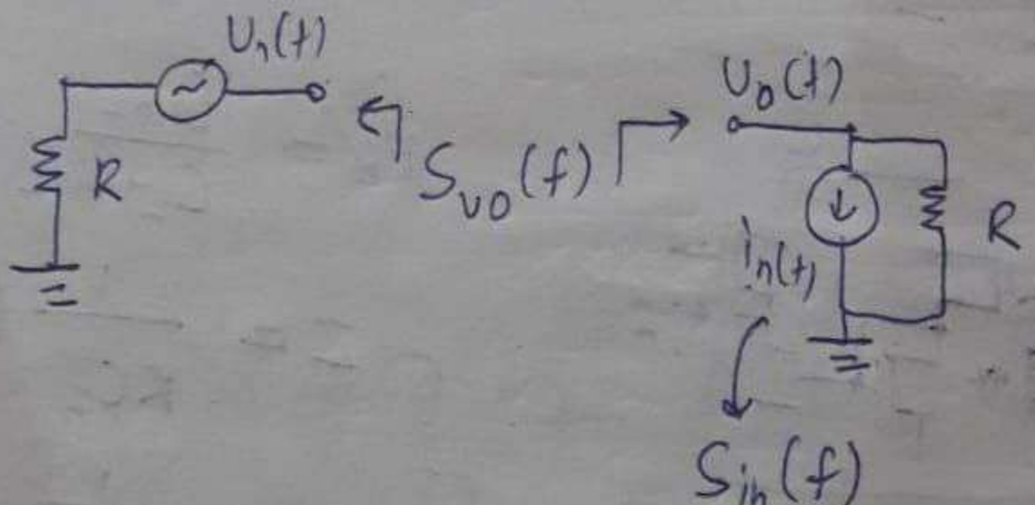
→ We have drop in $S_n$ at extremely high frequencies

It is constant in our frequencies of interest




When are the two representations equivalent?

↳ Both have the same effect.

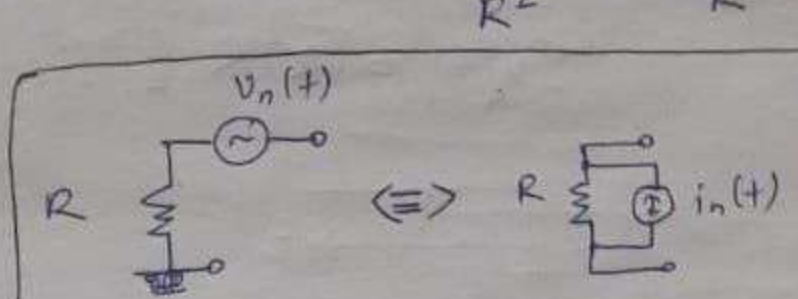


$V_o(t) = R I_n(t)$

$\Rightarrow S_y(f) = S_x(f)\,|H(f)|^2$

$\Rightarrow S_{vo}(f) = S_{in}(f) \times R^2 = 4kTR$

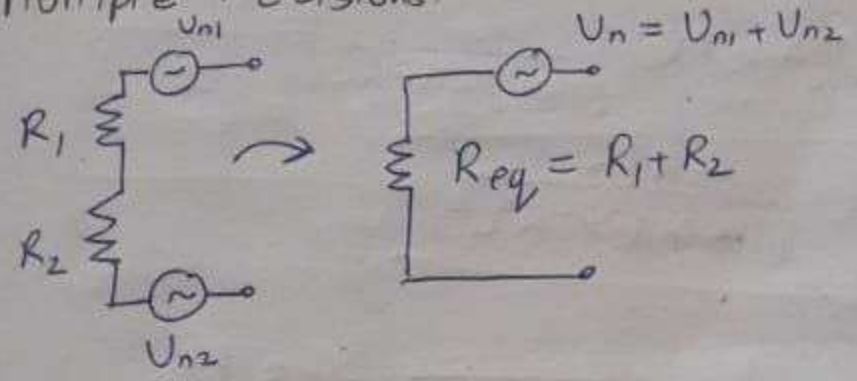
$\Rightarrow S_{in}(f) = \frac{4kTR}{R^2} = \frac{4kT}{R}$ $(A^2/Hz)$




$S_{v_n}(f) = 4kTR$

$S_{in}(f) = \frac{4kT}{R}$

- Multiple resistors:




$PSD_{eq}$ in terms of individual.

$PSD(R_1) = 4kTR_1$

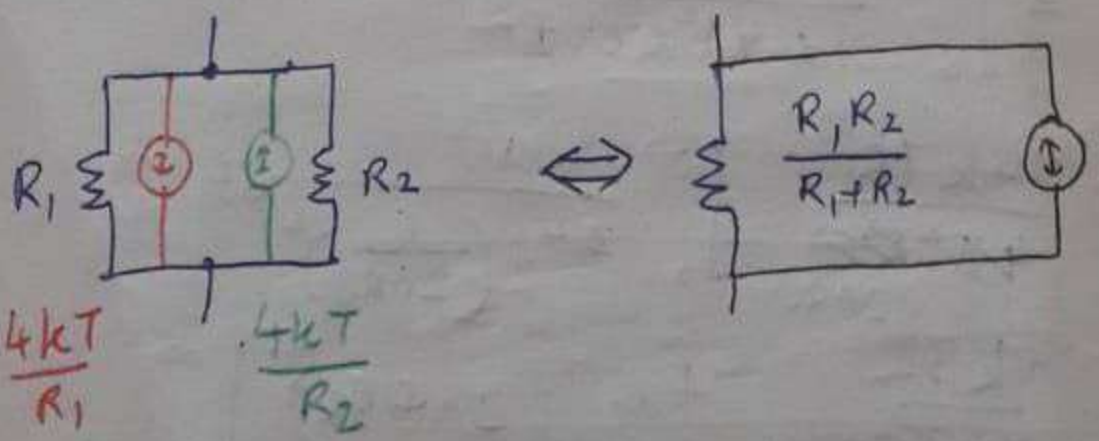
$PSD(R_2) = 4kTR_2$

Assuming $V_{n1}$, $V_{n2}$ are uncorrelated <independent resistors>

$\therefore PSD_{eq} = 4kTR_1 + 4kTR_2 = 4kT(R_1 + R_2)$

$$PSD_{series} = 4kT\left(\sum_i R_i\right)$$

In general, $\rightarrow PSD_{eq} = 4kT\,R_{eq}$ [Use for big circuits]




$PSD = \frac{4kT}{R_1} + \frac{4kT}{R_2}$

$= 4kT\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$

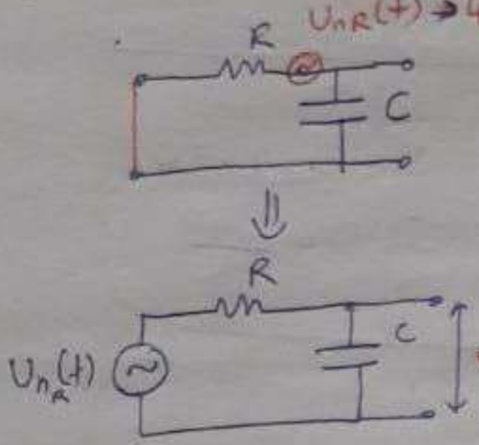
$= 4kT/R_{eq}$

$$S_{i\,net} = \frac{4kT}{R_{eq}} \qquad S_{v\,net} = 4kT\,R_{eq}$$

# Effect of Capacitor in Noise Analysis:

Capacitor → Doesn't produce noise
↳ Helps in noise shaping.

o PSD of RC ckt.



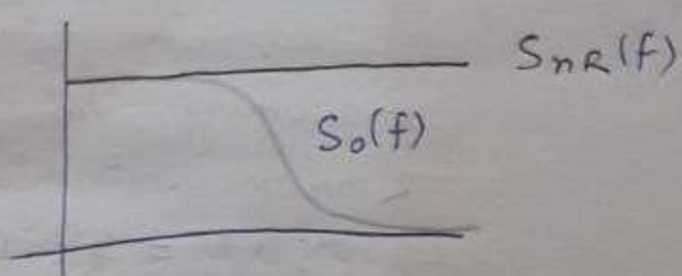

Noise analysis: $V_{in} = 0$

$S_{V_R}(f) = 4kTR$ [Input side]

$V_{on}(t) \rightarrow S_o(f) = S_{VR}(f)\,|H(f)|^2$

$$S_o(f) = (4kTR)\left|\frac{1}{1+j2\pi fRC}\right|^2$$

$$\boxed{S_o(f) = \frac{4kTR}{(1+4\pi^2 f^2 R^2 C^2)}}$$




Instead of visualising, engineers integrate to get power

$$P_{av} = \int_0^\infty S_o(f)\,df$$

$$= \int_0^\infty \frac{4kTR}{1+4\pi^2R^2C^2f^2}\,df$$

$$= \frac{4kTR}{4\pi^2R^2C^2}\int_0^\infty \frac{1}{f^2+\left(\frac{1}{2\pi RC}\right)^2}\,df$$

$$= \frac{4kTR}{\pi^2R^2C^2\,2\pi RC}\tan^{-1}(2\pi fRC)\Big|_0^\infty$$

$$= \frac{2kT}{\pi C}\times\frac{\pi}{2} = \frac{kT}{C} \rightarrow V^2$$

$$P_{av(R)} = \frac{kT}{C}$$ → Independent of C.

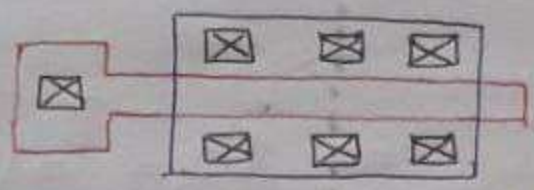
If R changes $S_V(f)$ shifts up by it decays a bit earlier.

Higher capacitor
↓ Better noise
↘ Poorer bandwidth
(Tradeoff)

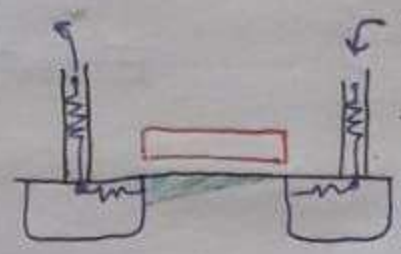
## Noise Sources in Circuits: Transistors

- Drain-Source Current Noise source (channel noise)

Assuming metal lines dont contribute to noise



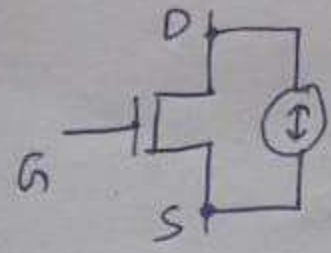
Cross-section




→ Contact resistors
- Come in parallel
- Reduce $R_{eq}$
→ PSD reduces.

→ Channel

↓ Works as a resistor
↓ Noise source




$$PSD\ (A^2/Hz) = \frac{4kT\gamma}{\left(\frac{1}{g_m}\right)} = 4kT\gamma g_m$$

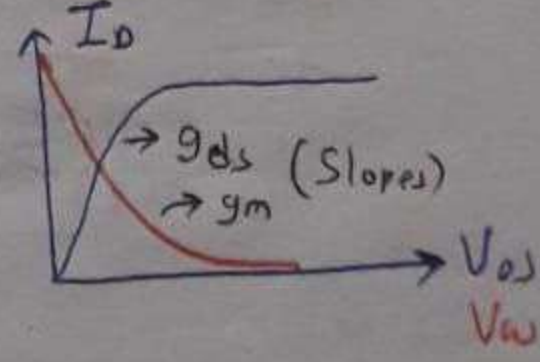
$R = \frac{1}{g_m}$ (why?)

$\gamma$ → Correction factor
↳ Depends on process

If channel is in triode → $R_{channel} = \frac{1}{g_{ds}} \rightarrow \frac{1}{g_m}$ [Deep Triode]

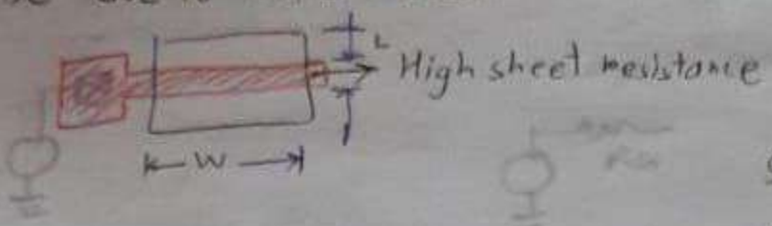
$$g_m(sat) = g_{ds}(deep\ triode)$$

PSD uses $g_m$ in sat.



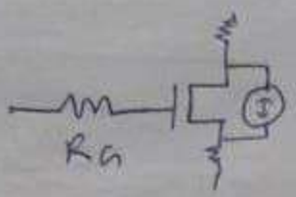

$$PSD_{channel} = 4kT\gamma g_m \ (A^2/Hz)$$

□ Noise due to Gate resistor

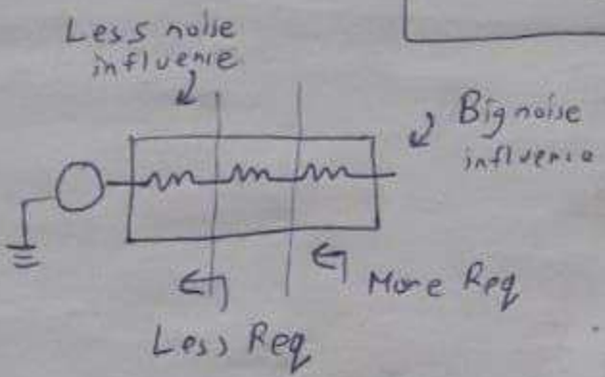



Sheet resistivity ($\Omega/\square$)

$$R_G' = \rho_\square \left(\frac{W}{L}\right)$$

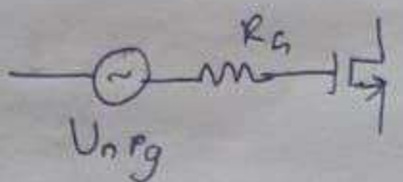



$$\boxed{R_G' = \rho_\square \left(\frac{W}{L}\right)}$$



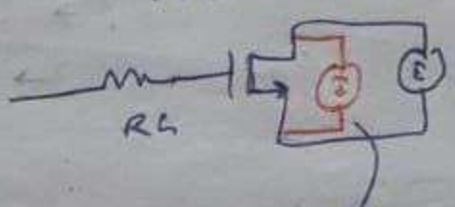

$$\Rightarrow \boxed{R_G = \rho_\square \left(\frac{W}{L}\right)\frac{1}{3}}$$

↓ Effective value




$\hookrightarrow PSD = 4kTR_G$

↓ Translate to current across DS



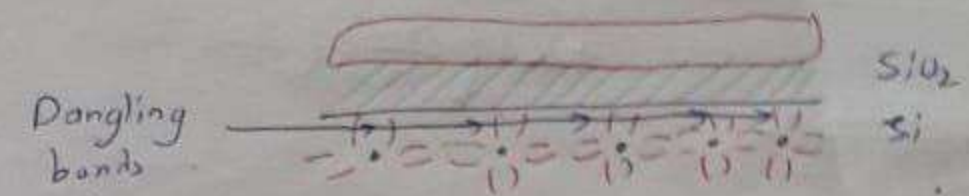

$\rightarrow 4kT\gamma g_m$

$$PSD = \underline{4kTR_G} \cdot \underline{g_m^2}$$

$S_{in} \qquad |H(f)|^2$

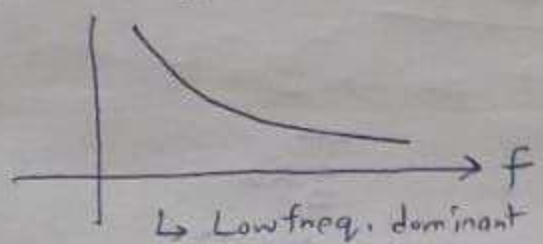
$$\boxed{PSD_{net} = 4kT(\gamma g_m + g_m^2 R_G)}$$

$$\boxed{R_G = \frac{1}{3}\rho_\square \frac{W}{L}}$$

□ Flicker noise

↳ Captures $e^-$s
(Halts / slows current

$\Leftarrow I_{DS} + i_n$

PSD $(i_n)/(V_n)$




↳ Low freq. dominant

We translate $i_n$ to Gate side

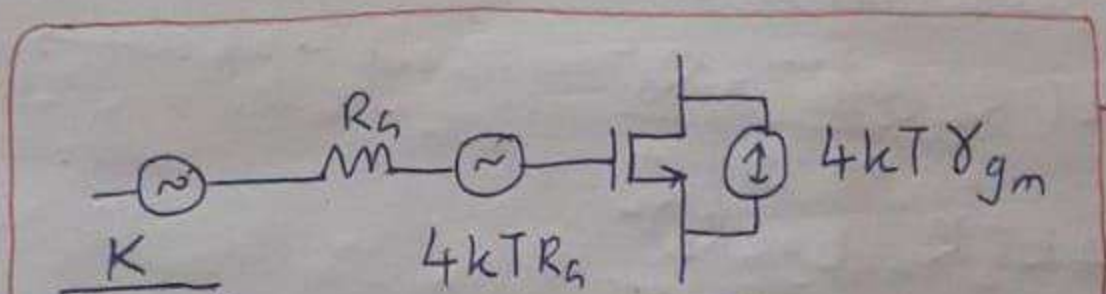
Also called 1/f noise

$$PSD\ (V^2/Hz) = \frac{K}{C_{ox} WL f}$$

net gate cap.

$$PSD\ (A^2/Hz) = \frac{K}{C_{ox} WLf} \cdot g_m^2$$

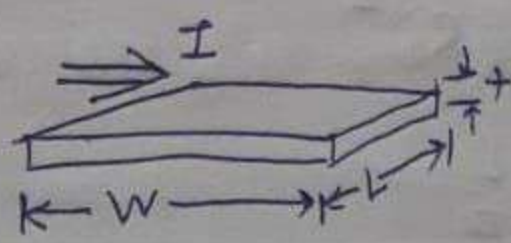
* PSD due to flicker noise $= \frac{K}{C_{ox} WL f} g_m^2$ $[A^2/Hz]$




→ 3 major noise components

$$R_G = \frac{1}{3} P_\square \frac{W}{L}$$

Sheet resistivity concept




$\rho$.

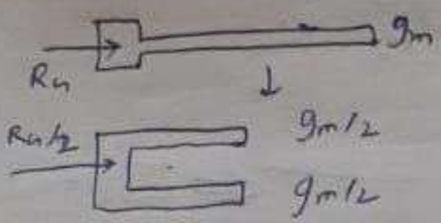
$$R = \rho \frac{W}{Lt}$$

$$R = \left(\frac{\rho}{t}\right)\left(\frac{W}{L}\right) = P_\square \frac{W}{L}$$

$$P_\square = \frac{\rho}{t} = \frac{1}{\sigma t}$$

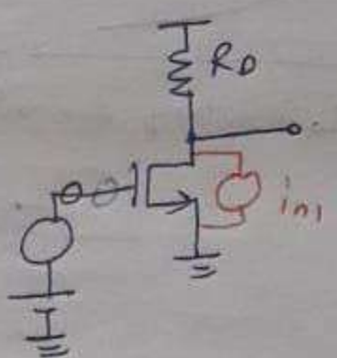
Splitting a transistor into n parts → reduce PSD by $\frac{1}{n^2}$

$$4kT\left(\frac{R_G}{n}\right)\left(\frac{g_m}{n}\right)^2 n$$




## Noise Analysis of CS Amplifier

- PSD of output noise voltage




- Due to Drain-Source channel noise [White]

$i_{n1} \rightarrow 4kT\gamma g_m \ (A^2/Hz)$

↓ I to V by $R_D$

$V_{n1} \rightarrow (4kT\gamma g_m)(R_D^2)$

$= 4kT\gamma g_m R_D^2$

↳ PSD of o/p noise due to channel noise

- Due to Gate resistor [White]

$4kT R_G (g_m)^2 \times R_D^2$ i/p volt. → o/p curr → o/p vol.

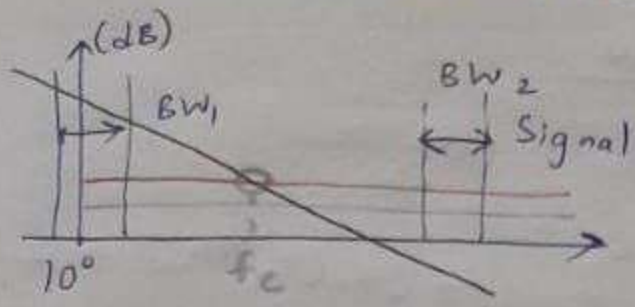
or

$\underbrace{4kT R_G}_{\text{i/p v.}} \underbrace{(g_m R_D)^2}_{\text{Voltage TF}=|H(f)|}$

- Due to flicker noise [Coloured]

$$\left(\frac{K}{C_{ox} WLf}\right)(g_m R_D)^2$$

i/p PSD volt. ↓ TF




Good design:
Red > Green

$\frac{1}{f}$ → becomes linear in log scale

Ignoring green, we compare red and black.

HF, RF → In the desired $BW_2$, channel noise is dominating.

Biomedical, sensor, energy harvesting → In the desired $BW_1$, flicker noise (1/f) is dominating.

What is low or high freq? → Compare with corner frequency $f_c$.

$f_c \rightarrow PSD_{flick} = PSD_{channel}$

$$\Rightarrow \frac{K}{WLC_{ox}} \frac{(g_m R_D)^2}{f_c} = 4kT\gamma g_m R_D^2$$

$$\Rightarrow f_c = \frac{K g_m^2 R_D^2}{4kT\gamma g_m R_D^2 WLC_{ox}}$$

$$\boxed{f_c = \frac{K g_m}{4k_B T WLC_{ox}}}$$

6 ~ 100 kHz → MHz

→ Depends on process

↳ Higher $f_c$, poorer process.

We can also consider noise due to $R_D$:

$$PSD(A^2/Hz) = \frac{4k_BT}{R_D}$$

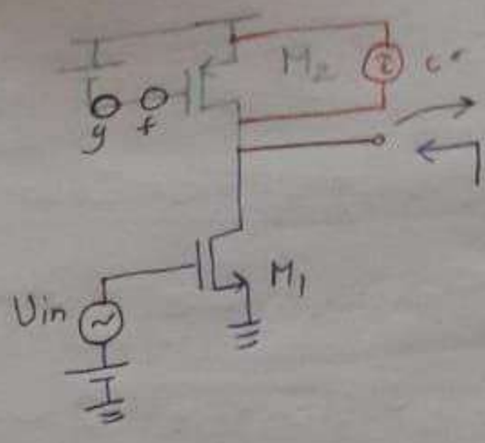
$$PSD(V^2/Hz) = 4k_BTR_D$$

Noise at o/p: (PSD, voltage form)

$$4k_BT\gamma g_m R_D^2 + 4k_BTR_S(g_mR_D)^2 + \frac{K(g_mR_D)^2}{C_{ox}WLf} + 4k_BTR_D$$

↳ Several factors degrading signal quality.

# CS amp. with active load




$V_{in}\, g_{m1}(r_{o1} \| r_{o2})$ → Signal

$R_o = r_{o1} \| r_{o2}$

$\text{Signal power} = V_{in}^2 g_{m1}^2 (r_{o1} \| r_{o2})^2$

o/p noise

↳ due to drain-source channel noise.

$$4kT\gamma g_{m2} \cdot (r_{o1} \| r_{o2})^2 \quad (M_2)$$
$$+4kT\gamma g_{m1} \cdot (r_{o1} \| r_{o2})^2 \quad (M_1)$$

↳ gate resistor

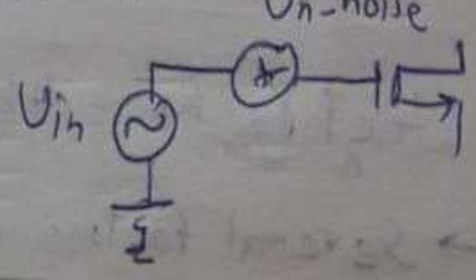
$$4kTR_{G_2}\left[g_{m2}(r_{o1} \| r_{o2})\right]^2 \quad (M_2)$$
$$+4kTR_{G_1}\left[g_{m1}(r_{o1} \| r_{o2})\right]^2 \quad (M_1)$$

↳ flicker noise

$$\frac{K_{M2}}{C_{ox} W_2 L_2} \cdot \frac{1}{f} \left(g_{m2}(r_{o1} \| r_{o2})\right)^2 \quad (M_2)$$
$$+ \frac{K_{M1}}{C_{ox} W_1 L_1} \cdot \frac{1}{f} \left(g_{m1}(r_{o1} \| r_{o2})\right)^2 \quad (M_1)$$

To get net noise power, add all the PSDs and integrate in band of interest.

We can translate the o/p noise into equivalent i/p voltage noise source



$$V^2_{out\_noise} = [g_{m1}(r_{o1} \| r_{o2})]^2 V^2_{in\_noise}$$

Input referred noise and input signal get amplified by same amount. Hence we use input referred noise more often.

$$\text{Input noise PSD} = \frac{PSD_{noise\_out}}{[g_{m1}(r_{o1} \| r_{o2})]^2}$$

$$V^2_{in\_noise} = \int (\text{input noise PSD}) \cdot df$$

↕

Compare with $V^2_{in}$-signal

For proper SNR, $V^2_{in}$-signal $\gg V^2_{in}$-noise

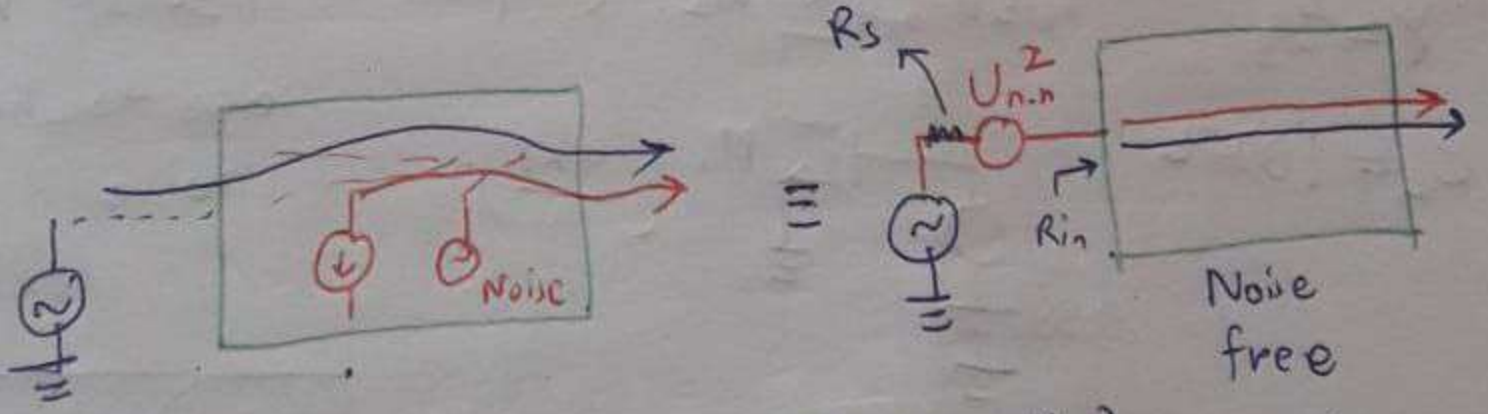
Circuit has to be designed so that $V^2_{in\_noise}$ is minimum; LNA design. [Gain is not a matter of concern, as both signal and noise undergo same amplification].

Music system → 8 bit equivalent

↳ $V_{sig} = 2^8 \times V_{noise}$

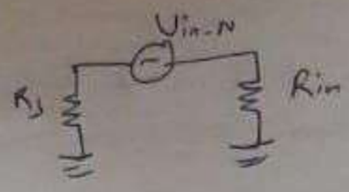
Bandwidth reduction → Also reduces noise

[10 kHz amp. → don't design 100 kHz amp. ∴
↳ Noise will kill system
↳ Customer gets pissed off. ☺ ]



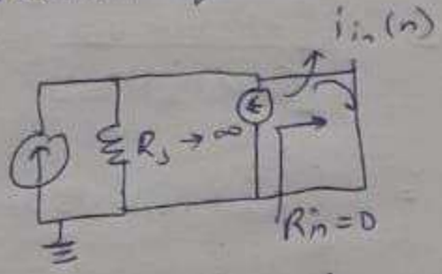

$R_s$ → small
$R_{in}$ → high
} assumption
↓
only then above rep. works

In case $R_s$ not small and $R_{in}$ → not high.



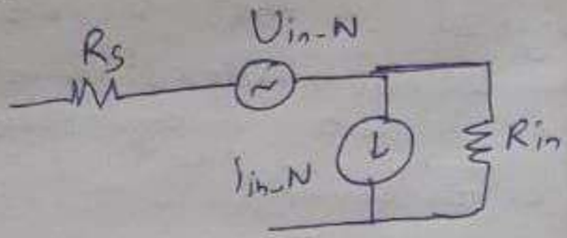

$V_{in-N} \frac{R_{in}}{R_{in}+R_s}$

Use Norton equivalent




For low $R_{in}$ → use $i_{in-n}$

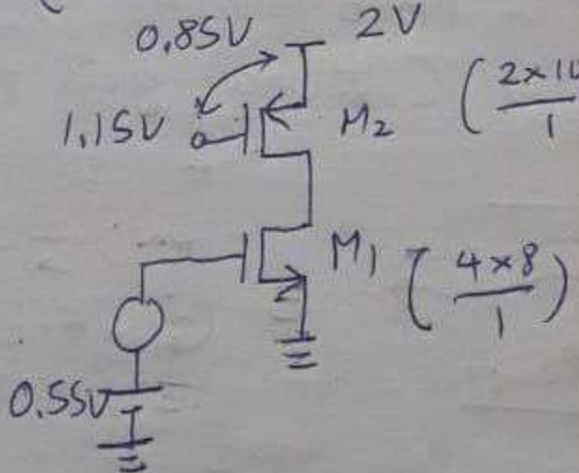
Best → use both models




Voltage stimulus → $i_{in-N}$ no contribution

Current stimulus → $V_{in-N}$ no contribution

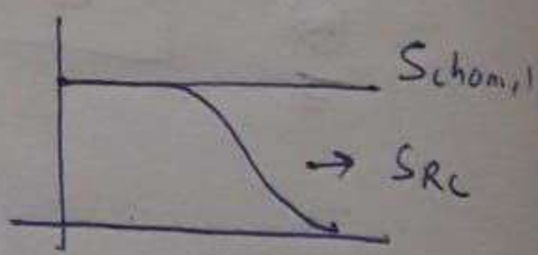
Numerical (3rd Test)




$\gamma = 2/3$

$C_L = 100fL$

PSD of $V_{o_N}$ due to channel noise




i/p ref noise voltage?

o/p noise power

K, $P_D$

* * *

END OF COURSE